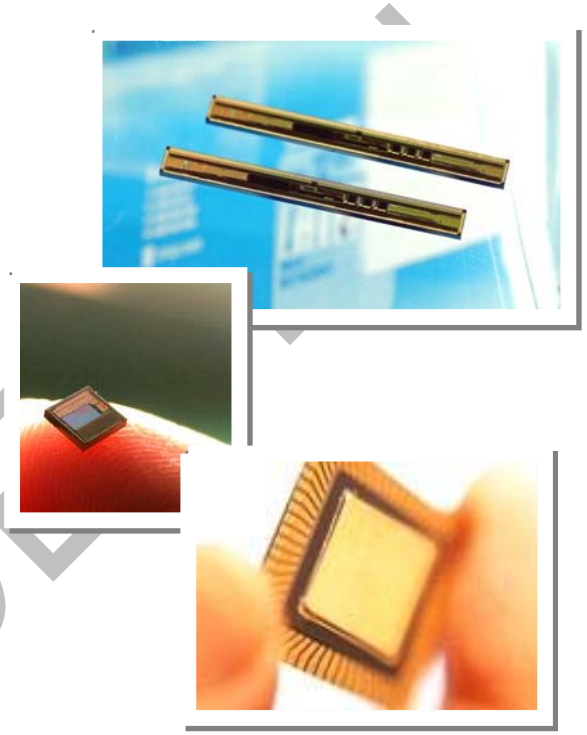
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation

Crystalfontz This controller datasheet was downloaded from **http://www.crystalfontz.com/controllers/**



# RM68120 Data Sheet

**Single Chip Driver with 16.7M color**

**for 480RGBx864 a-Si TFT LCD**

***Revision：0.0***

***Date：May 20, 2011***

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Revision History

| Version No. | Date | Page | Description |
|---|---|---|---|
| 0.0 | 2011/06/02 | P113 | Update OTP program flow chart |
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# 1. General Description

RM68120 is a 16.7 million-color single-chip SoC driver for a-si TFT LCD driver IC that supply resolution of 480RGBx360, 480RGBx640, 480RGBx720, 480RGBx800, 480RGBx854, 480RGBx864 with internal GRAM and 480RGB x 1024 by pass internal GRAM. RM68120 comprise a 1440-channel source driver, gate control timing by level shift, 1,244,160 bytes GRAM for graphic data of 480RGBx864 dots, and power supply circuit.

The RM68120 supports 24-/16-/8-bit data bus interface, I2C interface and serial peripheral interfaces (SPI). It also supplies 24bit, 18-bit or 16-bit RGB interface, MDDI interface and MIPI interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

RM68120 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving a TFT LCD panel. The RM68120 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the RM68120 an ideal driver for portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

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# 2. Features

- A single-chip controller driver for a WVGA panel type a-si TFT LCD display
- Display resolution option

  (1). With GRAM:

  1. 480RGB x 360
  2. 480RGB x 640
  3. 480RGB x 720
  4. 480RGB x 800
  5. 480RGB x 854
  6. 480RGB x 864

  (2). By pass GRAM:

  1. 480RGB x 1024
- RAM size: 480 x 3 x 864 = 1,244,160 bytes
- System interface

  (1). 8-, 16-, 24-bits 80-series MPU interface

  (2). 16-bits serial peripheral interface

  (3). I2C interface
- Moving picture display interface

  (1). 16-, 18-, 24-bit RGB interface (SYNC and DE mode)
- High speed interface

  (1). Mobile Display Digital Interface (MDDI V1.2, 1 clock and 1 or 2 data lane pairs)

  (2). MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
- Display color mode

  (1). Full color mode: 16.7M colors

  (2). Reduce color mode:

  1. 262k colors
  2. 65k colors

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3. 8 colors (Idle mode)

- Window address function to specify a rectangular area writing data in the internal RAM
- Abundant color display and drawing functions

  (1). Programmable γ-correction function for 16.7 million color display

  (2). Individual gamma correction setting for RGB dots

  (3). Partial display function
- Low power consumption architecture

  (1). Deep standby mode

  (2). Sleep mode

  (3). 8-color display function
- Power supply startup sequencer
- Support 1-, 2-, 3-, 4-dot, column and zigzag inversion
- Four GPO pins for external control
- On chip checksums check
- Operating temperate: -30℃ ~ 70℃
- On module DC/DC converter

  (1). DDVDH=4.5V to 6.5V

  (2). DDVDL=-4.5V to -6.5V

  (3). VCL=-2.5V to -4.0V

  (4). Positive gamma high voltage level: VGMP=3.5V to 5V

  (5). Positive gamma low voltage level: VGSP=0.0V, 0.3V to 3.7V

  (6). Negative gamma high voltage level: VGMN=-5V to -3.5V

  (7). Negative gamma low voltage level: VGSN=0.0V, -0.3V to -3.7V

  (8). Positive gate driver output voltage level: VGH=+8V to +18V

  (9). Negative gate driver output voltage level: VGL=-2V to -15V

  (10). VCOM=-3.5V to 0V
- Input power supply voltages:

  (1). IOVCC (VDDI) = 1.65V~3.3V

  (2). IOVCCL (VDDIL) = 1.1V~1.3V

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(3). VCI = 2.3V~4.8V

(4). MIPI/MDDI regulator supply voltage range: 2.3V ~ 4.8V

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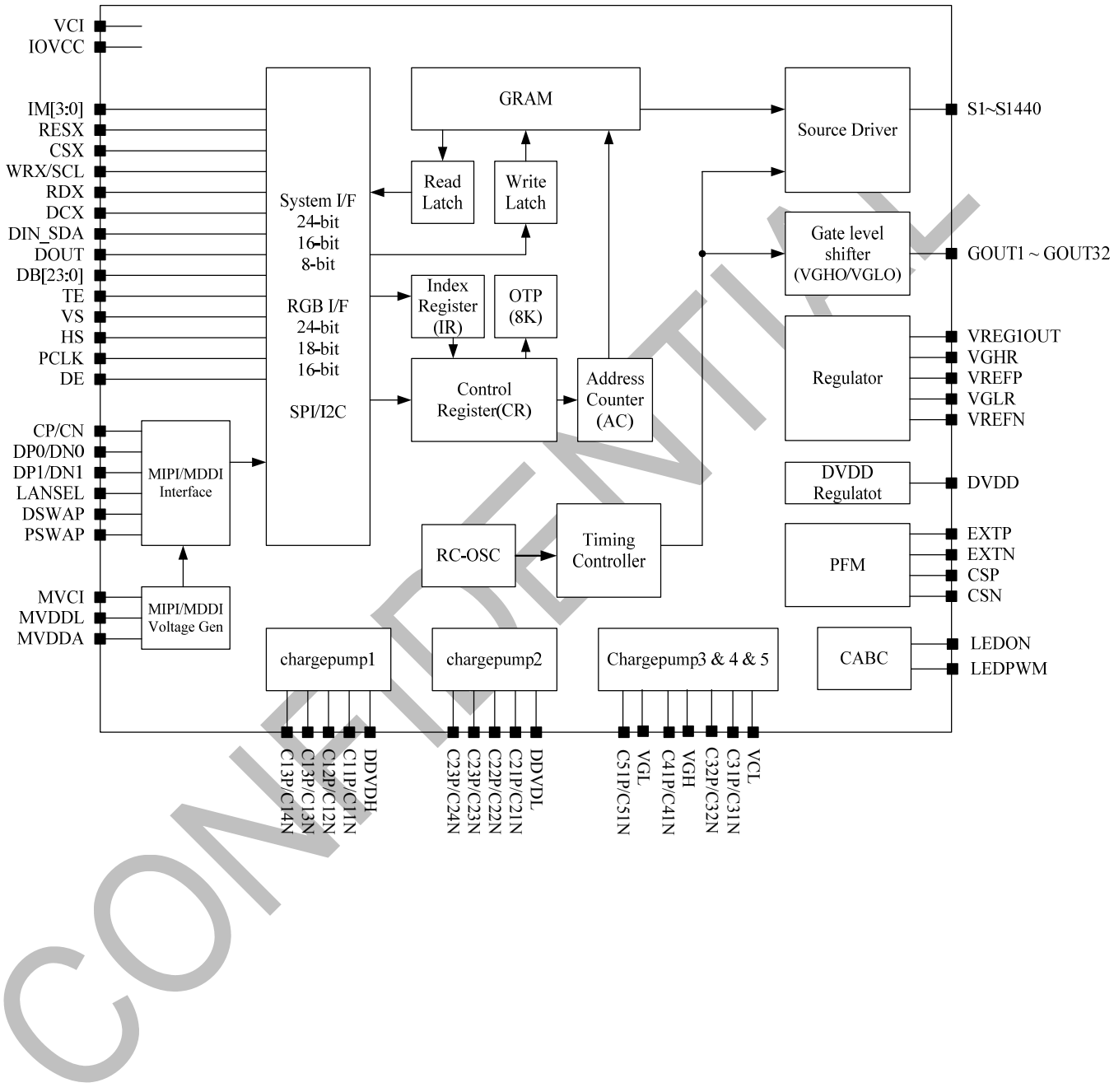
# 3. Block Diagram

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# 4. Pin Description

| 80-System Interface Pins | | |
|---|---|---|
| **Pin Name** | **I/O** | **Descriptions** |
| CSX | I | Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. |
| WRX / SCL / I2C_SCL | I | WRX: Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F.<br>SCL: A synchronous clock signal in SPI I/F.<br>I2C_SCL: Serial input clock in I2C I/F. |
| RDX | I | Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface. |
| D/CX | I | Display data / command selection in 80-series MPU I/F.<br>D/CX = ”0” : Command<br>D/CX = ”1” : Display data or Parameter |
| D[23:0] | I/O | 24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F.<br>For 8080-series MPU I/F:<br>8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI<br>16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI<br>24-bit interface: D[23:0] are used |
| **SPI / I2C Interface Pins** | | |
| **Pin Name** | **I/O** | **Descriptions** |
| SDI / I2C_SDA | I/O | SDI: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal.<br>I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. |
| SDO | O | Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. |
| **RGB Interface Pins** | | |
| **Pin Name** | **I/O** | **Descriptions** |
| PCLK | I | Pixel clock signal in RGB I/F. |
| VS | I | Vertical sync. Signal in RGB I/F. |
| HS | I | Horizontal sync. Signal in RGB I/F. |
| DE | I | Data enable signal in RGB I/F DE mode. |
| **MIPI / MDDI Interface Pins** | | |
| **Pin Name** | **I/O** | **Descriptions** |

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<table>
<tr><td>HSSI_CLK_P<br>HSSI_CLK_N</td><td>I</td><td>These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.<br>These pins are MDDI_STB_P/N differential strobe signals if MDDI interface is used.<br>HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.<br>Please connect these pins to VSSAM if not used.</td></tr>
<tr><td>HSSI_D0_P<br>HSSI_D0_N</td><td>I/O</td><td>These pins are DSI-D0+/- differential data signals if MIPI interface is used.<br>These pins are MDDI_DATA0_P/N differential strobe signals if MDDI interface is used.<br>HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.<br>Please connect these pins to VSSAM if not used.</td></tr>
<tr><td>HSSI_D1_P<br>HSSI_D1_N</td><td>I</td><td>These pins are DSI-D1+/- differential data signals if MIPI interface is used.<br>These pins are MDDI_DATA1_P/N differential strobe signals if MDDI interface is used.<br>HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.<br>Please connect these pins to VSSAM if not used.</td></tr>
<tr><td>ERR</td><td>O</td><td>CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found.<br>Please open this pin if not used.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface.<br>0: 1 data lane<br>1: 2 data lanes<br>Please connect to VSSI if not used.</td></tr>
<tr><td>DSWAP<br>PSWAP</td><td>I</td><td>Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.<br>For MIPI interface, both DSWAP and PSWAP function are available.<br>For MDDI interface, only PSWAP function is available. i.e. DSWAP=1 in below table is invalid.
<table>
<tr><th colspan="2">Pin Name</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th></tr>
<tr><td rowspan="4">MIPI/ MDDI</td><td>DSWAP=0<br>PSWAP=0</td><td>DSI-D0+</td><td>DSI-D0-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D1+</td><td>DSI-D1-</td></tr>
<tr><td>DSWAP=0<br>PSWAP=1</td><td>DSI-D0-</td><td>DSI-D0+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D1-</td><td>DSI-D1+</td></tr>
<tr><td>DSWAP=1<br>PSWAP=0</td><td>DSI-D1+</td><td>DSI-D1-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D0+</td><td>DSI-D0-</td></tr>
<tr><td>DSWAP=1<br>PSWAP=1</td><td>DSI-D1-</td><td>DSI-D1+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D0-</td><td>DSI-D0+</td></tr>
</table>
Please connect to VSSI if not used.</td></tr>
<tr><td colspan="3">Logic Pins</td></tr>
<tr><td>Pin Name</td><td>I/O</td><td>Descriptions</td></tr>
</table>

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<table>
<tr><td>RESX</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.
<table>
<tr><td colspan="2" rowspan="2">Input Voltage Level (DSTB_SEL=”1”)</td><td colspan="2">VDDI=1.65~3.3V</td><td colspan="2">VDDIL=1.1~1.3V</td></tr>
<tr><td>Min.</td><td>Max.</td><td>Min.</td><td>Max.</td></tr>
<tr><td rowspan="2">VSEL = 1</td><td>Logic high level input voltage</td><td>0.7xVDDI</td><td>VDDI</td><td>1.155</td><td>1.95</td></tr>
<tr><td>Logic low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td><td>VSSI</td><td>0.585</td></tr>
<tr><td rowspan="2">VSEL = 0</td><td>Logic high level input voltage</td><td>0.88</td><td>1.35</td><td>0.88</td><td>1.35</td></tr>
<tr><td>Logic low level input voltage</td><td>VSSI</td><td>0.55</td><td>VSSI</td><td>0.55</td></tr>
</table>
<table>
<tr><td colspan="2">Input Voltage Level (DSTB_SEL=”0”)</td><td>Min. (v)</td><td>Max. (v)</td></tr>
<tr><td rowspan="2">VDDI=1.65~3.3V</td><td>Logic High level input voltage</td><td>0.7xVDDI</td><td>VDDI</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td></tr>
<tr><td rowspan="2">VDDI=1.1~1.3V</td><td>Logic High level input voltage</td><td>0.88</td><td>1.35</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td></tr>
</table></td></tr>
<tr><td>TE_L</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.<br>Please open this pin if not used.</td></tr>
<tr><td>TE_R</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.<br>Please open this pin if not used.</td></tr>
<tr><td>RGBBP</td><td>I</td><td>Display data written path control in RGB interface.<br>RGBBP=”0”, display data written to frame memory.<br>RGBBP=”1”, display data written to line buffer (frame memory by pass mode)<br>Please connect to VSSI if not used in other interfaces.</td></tr>
</table>

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<table>
<tr>
<td>IM[3:0]</td>
<td>I</td>
<td>Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM[3:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>0000</td><td>80-series 8-bit MPU I/F, D[7:0]</td><td>80-series 8-bit MPU I/F, D[7:0]</td></tr>
<tr><td>0001</td><td>80-series 16-bit MPU I/F, D[15:0]</td><td>80-series 16-bit MPU I/F, D[15:0]</td></tr>
<tr><td>0010</td><td>80-series 24-bit MPU I/F, D[23:0]</td><td>80-series 24-bit MPU I/F, D[23:0]</td></tr>
<tr><td>0011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>0100</td><td>RGB I/F, D[23:0]</td><td>I2C I/F, I2C_SDA</td></tr>
<tr><td>0101</td><td>MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N</td><td>MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N</td></tr>
<tr><td>1101</td><td>MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N</td><td>MIPI DSI,HSSI_D0_P/N,HSSI_D1_P/N (Video Mode)</td></tr>
<tr><td>0110</td><td>MDDI,HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>1110</td><td>MDDI,HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0111</td><td>MDDI,HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>I2C I/F, I2C_SDA serial data</td></tr>
<tr><td>1011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
</table>
</td>
</tr>
<tr>
<td>I2C_SA</td>
<td>I</td>
<td>Select the I2C interface address from MPU.<br>0: 100_1100<br>1: 100_1101</td>
</tr>
</table>

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<table>
<tr><td>VSEL</td><td>I</td><td>Input pin to switch the I/O voltage.<br>This VSEL function only apply for RESX, TE, LEDPWM, LEDON, KBBC pins.<br>The VSEL dual IO function is valid when DSTB_SEL=”1”.<br><br>
<table>
<tr><td rowspan="2">DSTB_SEL</td><td rowspan="2">VDDI</td><td rowspan="2">VSEL</td><td rowspan="2">DIOPWR</td><td colspan="2">Output Voltage Level</td></tr>
<tr><td>TE</td><td>LEDON/LEDPWM</td></tr>
<tr><td>0</td><td>1.65~3.3v or<br>1.1~1.3v</td><td>X</td><td>Off</td><td>VOH=VDDI<br>VOL=VSSI</td><td>VOH=VDDI or VDDA<br>VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.65~3.3v</td><td>Low</td><td>1.2v</td><td>VOH=1.2v<br>VOL=VSSI</td><td>VOH=1.2<br>VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8v</td><td>VOH=VDDI<br>or DIOPWR<br>VOL=VSSI</td><td>VOH=VDDI or VDDA<br>VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.1~1.3v</td><td>Low</td><td>1.2v</td><td>VOH=1.2v<br>VOL=VSSI</td><td>VOH=1.2v<br>VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8v</td><td>VOH=1.8v<br>VOL=VSSI</td><td>VOH=1.8v<br>VOL=VSSI</td></tr>
</table>
The input voltage range for VSEL pin:
<table>
<tr><td>Input Voltage Level</td><td>Min.</td><td>Max.</td></tr>
<tr><td>Logic High level input voltage</td><td>0.88</td><td>VDDI</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td></tr>
</table>
Please open these pins if not used.</td></tr>
<tr><td>GPO[3:0]</td><td>O</td><td>General purpose output pins. The output voltage swing is VDDI to VSSI.</td></tr>
<tr><td>VGSW[3:0]</td><td>I</td><td>Input pin to select the different application.</td></tr>
<tr><td>EXB1T</td><td>I</td><td>Input pin to select the external DDVDH DC/DC voltage.<br>0: Use internal DC/DC for DDVDH<br>1: Use external DC/DC for DDVDH<br>Please connect to VSSI if not used.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>Input pin to select the voltage sequence of V0 ~ V255.<br>0: V(00h)>V(01h)>…>V(FEh)>V(FFh) (Normally White)<br>1: V(00h)<V(01h)<…<V(FEh)<V(FFh) (Normally Black)</td></tr>
<tr><td>DSTB_SEL</td><td>I</td><td>Input pin to control DIOPWR regulator on/off.
<table>
<tr><td>DSTB_SEL</td><td>DIOPWR Regulator</td><td>VSEL Function</td></tr>
<tr><td>0</td><td>DIOPWR Off</td><td>Invalid</td></tr>
<tr><td>1</td><td>DIOPWR On</td><td>Valid</td></tr>
</table></td></tr>
<tr><td colspan="3">CABC and LABC Pins</td></tr>
<tr><td>Pin Name</td><td>I/O</td><td>Descriptions</td></tr>
<tr><td>LEDON</td><td>O</td><td>This pin is connect to the external LED driver.<br>It is a LED driver control signal which is used for turning ON/OFF the LED backlight.</td></tr>
</table>

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| | | |
|---|---|---|
| LEDPWM | O | This pin is connect to the external LED driver.<br>It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High). |

## Power supply

| Pin Name | I/O | Descriptions |
|---|---|---|
| VDDB | DC/DC Power | Power supply for DC/DC converter<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDDA | Analog Power | Power supply for analog system<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDDR | Regulator Power | Power supply for regulator system<br>VDDB, VDDA and VDDR should be the same input voltage level |
| VDD_DET | Detection Power | Connect to VDDB/VDDA/VDDR for detection. |
| VDDAM | MIPI Power | Power supply for MIPI/MDDI analog regulator system |
| VDDI | I/O Power | Power supply for interface system except MIPI/MDDI interface |
| DVDD | Digital Voltage | Regulator output for logic system power (1.5V typical)<br>Connect a capacitor for stabilization. |
| DIOPWR | Dual I/O Voltage | Regulator output for dual I/O voltage system (1.2V/1.8V typical).<br>Connect a capacitor for stabilization. |
| MVDDA | MIPI/MDDI Voltage | Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization.<br>If not use MIPI/MDDI interface, please open this pin. |
| MVDDL | MIPI Voltage | Regulator output for internal MIPI low power system (1.2V typical)<br>Connect a capacitor for stabilization.<br>If not use MIPI interface, please open this pin |
| VSSB | DC/DC GND | System ground for DC/DC converter |
| VSSA | Analog GND | System ground for analog system |
| VSSR | Regulator GND | System ground for regulator system |
| VSSAM | MIPI GND | System ground for internal MIPI/MDDI analog system |
| VSSI | I/O GND | System ground for interface system except MIPI/MDDI interface |

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| | | |
|---|---|---|
| DVSS | Digital GND | System ground for internal digital system |
| AVSS | Source OP GND | System ground for source OP system |
| MTP_PWR | MTP Power | MTP programming power supply pin (7.4 to 7.6V and 7.5V typical) Must be left open or connected to DVSS in normal condition |

## Step-up Circuit

| Pin Name | I/O | Descriptions |
|---|---|---|
| AVDD (DDVDH) | O | Output voltage from step-up circuit 1, generated from VDDB.<br>Connect a capacitor for stabilization. |
| AVEE (DDVDL) | O | Output voltage from step-up circuit 2, generated from VDDB.<br>Connect a capacitor for stabilization. |
| VCL | O | Output voltage from step-up circuit 3, generated from VDDB.<br>Connect a capacitor for stabilization. |
| VGH | O | Output voltage from step-up circuit 4.<br>Connect a capacitor for stabilization. |
| VGLX | O | Output voltage from step-up circuit 5.<br>Connect a capacitor for stabilization. |
| VGL | I | Substrate voltage for driver IC. Please connect VGL to VGLX. |
| C11P, C11N<br>C12P, C12N<br>C13P, C13N<br>C14P, C14N | O | Capacitor connection pins for the step-up circuit which generate AVDD.<br>Connect capacitor as requirement. |
| C21P, C21N<br>C22P, C22N<br>C23P, C23N<br>C24P, C24N | O | Capacitor connection pins for the step-up circuit which generate AVEE.<br>Connect capacitor as requirement. |
| C31P, C31N<br>C32P, C32N | O | Capacitor connection pins for the step-up circuit which generate VCL.<br>Connect capacitor as requirement. |
| C41P, C41N | O | Capacitor connection pins for the step-up circuit which generate VGH.<br>Connect capacitor as requirement. |
| C51P, C51N | O | Capacitor connection pins for the step-up circuit which generate VGLX.<br>Connect capacitor as requirement. |
| VRGH | O | Output voltage generated from AVDD.<br>Connect a capacitor for stabilization. |
| VGL_REG | O | Output voltage generated from VGLX. LDO output used for panel voltage.<br>Connect a capacitor for stabilization. |

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| | | |
|---|---|---|
| EXTP | O | PFM1 control output for DC/DC converter to generate AVDD.<br>Connect to gate of external NMOS device. |
| EXTN | O | PFM2 control output for DC/DC converter to generate AVEE.<br>Connect to gate of external PMOS device. |
| CSP | I | Current sensing input for PFM1 DC/DC converter (generate AVDD). |
| CSN | I | Current sensing input for PFM2 DC/DC converter (generate AVEE). |
| VREF_PWR | O | Regulator output for power voltage.<br>Connect a capacitor for stabilization. |
| VREFCP | O | Reference voltage for internal voltage generating circuit.<br>Connect capacitor for stabilization. |
| VGMP | O | Output voltage generated from AVDD. LDO output for positive gamma high voltage generator. |
| VGSP | O | Output voltage generated from AVDD. LDO output for positive gamma low voltage generator. |
| VGMN | O | Output voltage generated from AVEE. LDO output for negative gamma high voltage generator. |
| VGSN | O | Output voltage generated from AVEE. LDO output for negative gamma low voltage generator. |
| **Output Pins** | | |
| **Pin Name** | **I/O** | **Descriptions** |
| S1 ~S1440 | O | Pixel electrode driving output. |
| GOUT1 ~ GOUT32 | O | Gate control signals for panel.<br>The swing voltage level is VGHO to VGLO |
| SDUM0 ~ 3 | O | Dummy Source. |
| VGHO | O | High voltage level for gate control signals and gate circuit of panel. |
| VGLO | O | Low voltage level for gate control signals and gate circuit of panel. |
| LVGL | O | Low voltage level for gate circuit of panel. |
| VCOM | O | Regulator output for common voltage of panel.<br>Connect a capacitor for stabilization. |
| **Test and Dummy pins** | | |
| **Pin Name** | **I/O** | **Descriptions** |

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| | | |
|---|---|---|
| PADA1<br>PADA2<br>PADA3<br>PADA4<br>PADB1<br>PADB2<br>PADB3<br>PADB4 | I/O | These test pins for chip attachment detection.<br>PADA1 to PADA4 are output pins and PADB1 to PADB4 are input pins.<br>For normal operation:<br>Connect PADA1 and PADB1 together by ITO trace.<br>Connect PADA2 and PADB2 together by ITO trace.<br>Connect PADA3 and PADB3 together by ITO trace.<br>Connect PADA4 and PADB4 together by ITO trace. |
| CONTACT1A,<br>CONTACT1B,<br>CONTACT2A,<br>CONTACT2B | I/O | Test pin, for test bonding quality, IC internal will connect<br>CONTACT1A with CONTACT1B, CONTACT2A with CONTACT2B |
| AVSS_AVDD | I | Test pin, must be connected to AVSS |
| AVEE_AVSS | I | Test pin, must be connected to AVEE |
| VCL_VDDB | I | Test pin, must be connected to VCL |
| VCL_AVSS | I | Test pin, must be connected to VCL |
| VGMN_VGMP | I | Test pin, must be connected to VGMN |
| VGSN_VGSP | I | Test pin, must be connected to VGSN |
| KBBC | I | Test pin, not accessible to user. |
| TEST0~7 | I/O | Test pin, not accessible to user. Must be left open. |
| OSC_TEST | I/O | Test pin, not accessible to user, Must left open |
| VDDI_OPT1~2 | O | Use them to fix the electrical potentials of unused interface pins and fixed pins. |
| VSSI_OPT1 | O | Use them to fix the electrical potentials of unused interface pins and fixed pins. |
| VSSIDUM0~106 | O | These pins are dummy with VSSI potential (not have any function inside).<br>Signal traces can’t pass through on glass under these pads. |

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**A-Si TFT LCD Drive Power Supply Specifications Table**

| No. | Item | | Description |
|---|---|---|---|
| 1 | TFT source driver | | 1440 pins (S1 ~ S1440) |
| 2 | TFT gate driver | | 32 pins (GOUT1 ~ GOUT32) |
| 3 | Liquid crystal drive output | S1~S1440 | V0~V255 grayscales |
| | | GOUT1 ~ GOUT32 | VGH-VGL |
| | | VCOM | DC VCOM |
| 4 | Input voltage | IOVCC | 1.65V~3.30V |
| | | VCI | 2.30V~4.80V |
| 5 | Liquid crystal drive voltages | DDVDH | 4.5V ~ 6.5V |
| | | DDVDL | -4.5V ~ -6.5V |
| | | VGH | 8.0V ~ 18V |
| | | VGL | -2V ~ -15V |
| | | VGH-VGL | Avoid exceed 32v |
| 6 | Internal step-up circuits | DDVDH | VCIx1.5, VCIx1.66, VCIx2, VCIx2.5, VCIx3 |
| | | DDVDL | VCIx-1.5, VCIx-2, VCIx-2.5, VCIx-3 |
| | | VCL | VCIx-0.5, VCIx-1.0, VCIx-2.0 |
| | | VGH | (DDVDH+VCI), DDVDHx2, (DDVDH-DDVDL+VCI), (DDVDHx2-DDVDL) |
| | | VGLX | (DDVDL+VCL), (DDVDL-DDVDH), (DDVDL+VCL-DDVDH), (DDVDLx2 – DDVDH) |

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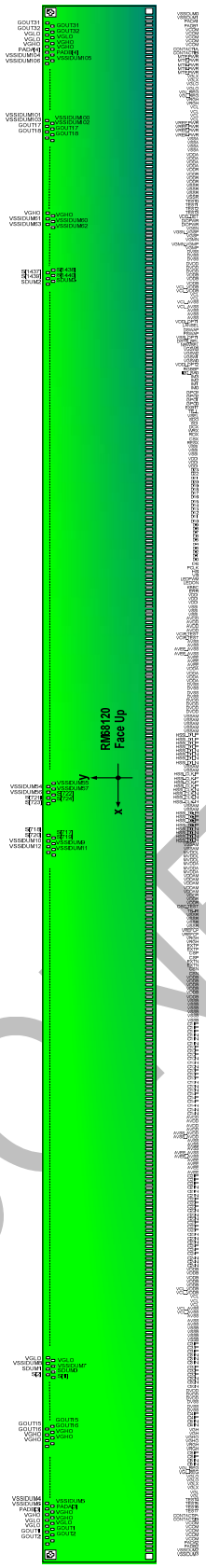
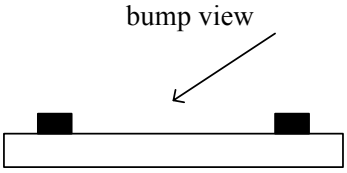
# 5. Pad Diagram and Coordination

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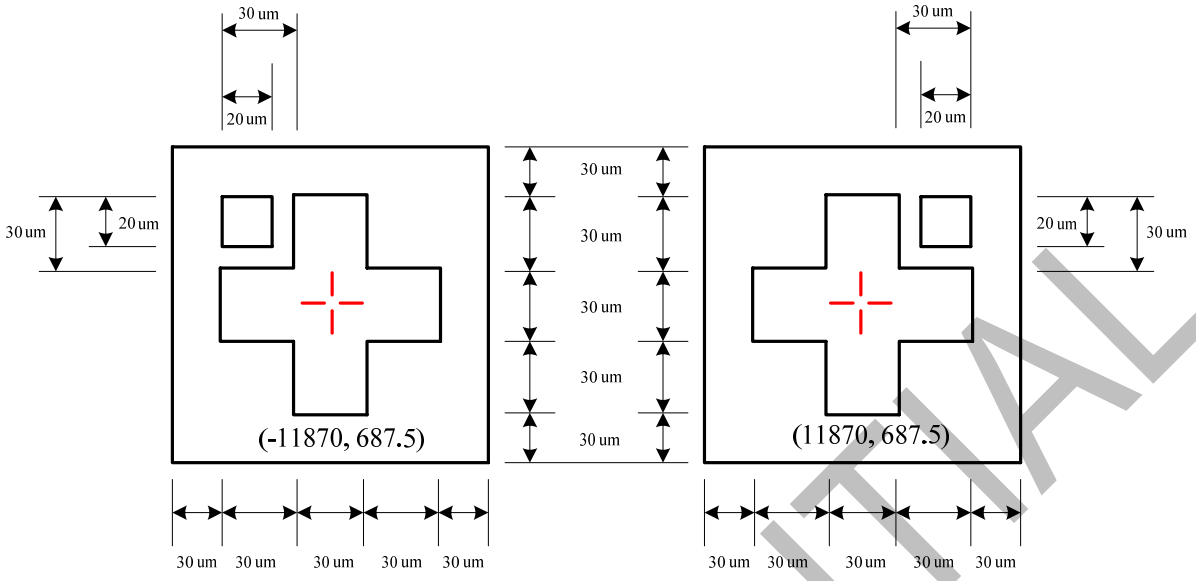
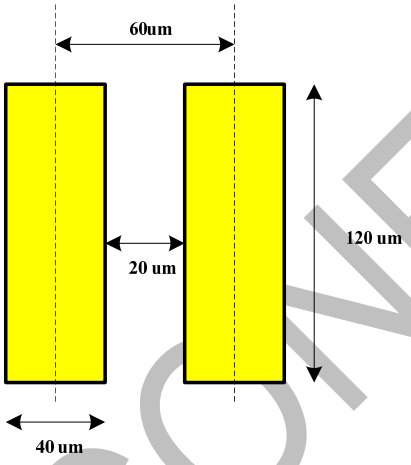
**Alignment Mark:**



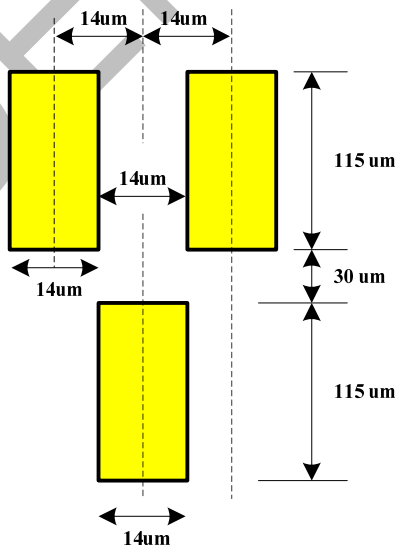

**Bump Arrangment:**

**Input:**




Input Pad

**Output:**




Output Pad

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**Coordinate:**

| Pad No. | Name | X-axis | Y-axis |
|---|---|---|---|
| 1 | VSSIDUM0 | -11880 | -702.5 |
| 2 | VSSIDUM1 | -11790 | -702.5 |
| 3 | PADA1 | -11730 | -702.5 |
| 4 | PADB1 | -11670 | -702.5 |
| 5 | VCOM | -11610 | -702.5 |
| 6 | VCOM | -11550 | -702.5 |
| 7 | VCOM | -11490 | -702.5 |
| 8 | VCOM | -11430 | -702.5 |
| 9 | VCOM | -11370 | -702.5 |
| 10 | CONTACT1A | -11310 | -702.5 |
| 11 | CONTACT1B | -11250 | -702.5 |
| 12 | MTP_PWR | -11190 | -702.5 |
| 13 | MTP_PWR | -11130 | -702.5 |
| 14 | MTP_PWR | -11070 | -702.5 |
| 15 | MTP_PWR | -11010 | -702.5 |
| 16 | MTP_PWR | -10950 | -702.5 |
| 17 | VGLX | -10890 | -702.5 |
| 18 | VGLX | -10830 | -702.5 |
| 19 | VGLO | -10770 | -702.5 |
| 20 | VGLO | -10710 | -702.5 |
| 21 | VGL_REG | -10650 | -702.5 |
| 22 | VGL_REG | -10590 | -702.5 |
| 23 | VRGH | -10530 | -702.5 |
| 24 | VRGH | -10470 | -702.5 |
| 25 | VCL | -10410 | -702.5 |
| 26 | VCL | -10350 | -702.5 |
| 27 | VCL | -10290 | -702.5 |
| 28 | VCL | -10230 | -702.5 |
| 29 | VREF_PWR | -10170 | -702.5 |
| 30 | VREF_PWR | -10110 | -702.5 |
| 31 | VREF_PWR | -10050 | -702.5 |
| 32 | VREF_PWR | -9990 | -702.5 |
| 33 | VSSA | -9930 | -702.5 |
| 34 | VSSA | -9870 | -702.5 |
| 35 | VSSA | -9810 | -702.5 |
| 36 | VSSA | -9750 | -702.5 |
| 37 | VDDA | -9690 | -702.5 |
| 38 | VDDA | -9630 | -702.5 |
| 39 | VDDA | -9570 | -702.5 |
| 40 | VDDA | -9510 | -702.5 |
| 41 | VDDR | -9450 | -702.5 |
| 42 | VDDR | -9390 | -702.5 |
| 43 | VDDR | -9330 | -702.5 |
| 44 | VDDR | -9270 | -702.5 |
| 45 | VSSR | -9210 | -702.5 |
| 46 | VSSR | -9150 | -702.5 |
| 47 | VSSR | -9090 | -702.5 |
| 48 | VSSR | -9030 | -702.5 |
| 49 | TEST0 | -8970 | -702.5 |
| 50 | TEST1 | -8910 | -702.5 |
| 51 | TEST2 | -8850 | -702.5 |
| 52 | TEST3 | -8790 | -702.5 |
| 53 | VDD_DET | -8730 | -702.5 |
| 54 | DIOPWR | -8670 | -702.5 |
| 55 | DIOPWR | -8610 | -702.5 |
| 56 | VGSN | -8550 | -702.5 |
| 57 | VGSN_VGSP | -8490 | -702.5 |
| 58 | VGSP | -8430 | -702.5 |
| 59 | VGMN | -8370 | -702.5 |
| 60 | VGMN_VGMP | -8310 | -702.5 |
| 61 | VGMP | -8250 | -702.5 |
| 62 | DVSS | -8190 | -702.5 |
| 63 | DVSS | -8130 | -702.5 |
| 64 | DVSS | -8070 | -702.5 |
| 65 | DVDD | -8010 | -702.5 |
| 66 | DVDD | -7950 | -702.5 |
| 67 | DVDD | -7890 | -702.5 |
| 68 | VDDB | -7830 | -702.5 |
| 69 | VDDB | -7770 | -702.5 |
| 70 | VDDB | -7710 | -702.5 |
| 71 | VCL_VDDB | -7650 | -702.5 |
| 72 | VCL_VDDB | -7590 | -702.5 |
| 73 | VCL | -7530 | -702.5 |
| 74 | VCL | -7470 | -702.5 |
| 75 | VCL_AVSS | -7410 | -702.5 |
| 76 | VCL_AVSS | -7350 | -702.5 |
| 77 | AVSS | -7290 | -702.5 |
| 78 | AVSS | -7230 | -702.5 |
| 79 | AVSS | -7170 | -702.5 |
| 80 | VDDI_OPT1 | -7110 | -702.5 |
| 81 | LANSEL | -7050 | -702.5 |
| 82 | DSWAP | -6990 | -702.5 |
| 83 | PSWAP | -6930 | -702.5 |
| 84 | VSSI_OPT1 | -6870 | -702.5 |
| 85 | DSTB_SEL | -6810 | -702.5 |
| 86 | NBWSEL | -6750 | -702.5 |
| 87 | VGSW3 | -6690 | -702.5 |
| 88 | VGSW2 | -6630 | -702.5 |
| 89 | VGSW1 | -6570 | -702.5 |
| 90 | VGSW0 | -6510 | -702.5 |
| 91 | VDDI_OPT2 | -6450 | -702.5 |
| 92 | RGBBP | -6390 | -702.5 |
| 93 | I2C_SA0 | -6330 | -702.5 |
| 94 | IM3 | -6270 | -702.5 |
| 95 | IM2 | -6210 | -702.5 |
| 96 | IM1 | -6150 | -702.5 |
| 97 | IM0 | -6090 | -702.5 |
| 98 | GPO3 | -6030 | -702.5 |
| 99 | GPO2 | -5970 | -702.5 |
| 100 | GPO1 | -5910 | -702.5 |
| 101 | GPO0 | -5850 | -702.5 |
| 102 | EXB1T | -5790 | -702.5 |
| 103 | TE_L | -5730 | -702.5 |
| 104 | VSEL | -5670 | -702.5 |
| 105 | SDO | -5610 | -702.5 |
| 106 | SDI | -5550 | -702.5 |
| 107 | DCX | -5490 | -702.5 |
| 108 | WRX | -5430 | -702.5 |
| 109 | RDX | -5370 | -702.5 |
| 110 | CSX | -5310 | -702.5 |
| 111 | RESX | -5250 | -702.5 |

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| | | | |
|---|---|---|---|
| 112 | VSSI | -5190 | -702.5 |
| 113 | VSSI | -5130 | -702.5 |
| 114 | VSSI | -5070 | -702.5 |
| 115 | VDDI | -5010 | -702.5 |
| 116 | VDDI | -4950 | -702.5 |
| 117 | VDDI | -4890 | -702.5 |
| 118 | D23 | -4830 | -702.5 |
| 119 | D22 | -4770 | -702.5 |
| 120 | D21 | -4710 | -702.5 |
| 121 | D20 | -4650 | -702.5 |
| 122 | D19 | -4590 | -702.5 |
| 123 | D18 | -4530 | -702.5 |
| 124 | D17 | -4470 | -702.5 |
| 125 | D16 | -4410 | -702.5 |
| 126 | D15 | -4350 | -702.5 |
| 127 | D14 | -4290 | -702.5 |
| 128 | D13 | -4230 | -702.5 |
| 129 | D12 | -4170 | -702.5 |
| 130 | D11 | -4110 | -702.5 |
| 131 | D10 | -4050 | -702.5 |
| 132 | D9 | -3990 | -702.5 |
| 133 | D8 | -3930 | -702.5 |
| 134 | D7 | -3870 | -702.5 |
| 135 | D6 | -3810 | -702.5 |
| 136 | D5 | -3750 | -702.5 |
| 137 | D4 | -3690 | -702.5 |
| 138 | D3 | -3630 | -702.5 |
| 139 | D2 | -3570 | -702.5 |
| 140 | D1 | -3510 | -702.5 |
| 141 | D0 | -3450 | -702.5 |
| 142 | DE | -3390 | -702.5 |
| 143 | PCLK | -3330 | -702.5 |
| 144 | HS | -3270 | -702.5 |
| 145 | VS | -3210 | -702.5 |
| 146 | LEDPWM | -3150 | -702.5 |
| 147 | LEDON | -3090 | -702.5 |
| 148 | KBBC | -3030 | -702.5 |
| 149 | ERR | -2970 | -702.5 |
| 150 | VDDI | -2910 | -702.5 |
| 151 | VDDI | -2850 | -702.5 |
| 152 | VDDI | -2790 | -702.5 |
| 153 | VSSI | -2730 | -702.5 |
| 154 | VSSI | -2670 | -702.5 |
| 155 | VSSI | -2610 | -702.5 |
| 156 | AVDD | -2550 | -702.5 |
| 157 | AVDD | -2490 | -702.5 |
| 158 | AVDD | -2430 | -702.5 |
| 159 | AVDD | -2370 | -702.5 |
| 160 | AVSS_AVDD | -2310 | -702.5 |
| 161 | AVSS_AVDD | -2250 | -702.5 |
| 162 | AVSS | -2190 | -702.5 |
| 163 | AVSS | -2130 | -702.5 |
| 164 | AVEE_AVSS | -2070 | -702.5 |
| 165 | AVEE_AVSS | -2010 | -702.5 |
| 166 | AVEE | -1950 | -702.5 |
| 167 | AVEE | -1890 | -702.5 |
| 168 | AVEE | -1830 | -702.5 |
| 169 | VDDA | -1770 | -702.5 |
| 170 | VDDA | -1710 | -702.5 |
| 171 | VDDA | -1650 | -702.5 |
| 172 | VDDA | -1590 | -702.5 |
| 173 | DVSS | -1530 | -702.5 |
| 174 | DVSS | -1470 | -702.5 |
| 175 | DVSS | -1410 | -702.5 |
| 176 | DVSS | -1350 | -702.5 |
| 177 | DVDD | -1290 | -702.5 |
| 178 | DVDD | -1230 | -702.5 |
| 179 | DVDD | -1170 | -702.5 |
| 180 | DVDD | -1110 | -702.5 |
| 181 | VSSAM | -1050 | -702.5 |
| 182 | VSSAM | -990 | -702.5 |
| 183 | VSSAM | -930 | -702.5 |
| 184 | VSSAM | -870 | -702.5 |
| 185 | VSSAM | -810 | -702.5 |
| 186 | HSSI_D1_P | -750 | -702.5 |
| 187 | HSSI_D1_P | -690 | -702.5 |
| 188 | HSSI_D1_P | -630 | -702.5 |
| 189 | HSSI_D1_P | -570 | -702.5 |
| 190 | HSSI_D1_N | -510 | -702.5 |
| 191 | HSSI_D1_N | -450 | -702.5 |
| 192 | HSSI_D1_N | -390 | -702.5 |
| 193 | HSSI_D1_N | -330 | -702.5 |
| 194 | VSSAM | -270 | -702.5 |
| 195 | VSSAM | -210 | -702.5 |
| 196 | HSSI_CLK_P | -150 | -702.5 |
| 197 | HSSI_CLK_P | -90 | -702.5 |
| 198 | HSSI_CLK_P | -30 | -702.5 |
| 199 | HSSI_CLK_P | 30 | -702.5 |
| 200 | HSSI_CLK_N | 90 | -702.5 |
| 201 | HSSI_CLK_N | 150 | -702.5 |
| 202 | HSSI_CLK_N | 210 | -702.5 |
| 203 | HSSI_CLK_N | 270 | -702.5 |
| 204 | VSSAM | 330 | -702.5 |
| 205 | VSSAM | 390 | -702.5 |
| 206 | HSSI_D0_P | 450 | -702.5 |
| 207 | HSSI_D0_P | 510 | -702.5 |
| 208 | HSSI_D0_P | 570 | -702.5 |
| 209 | HSSI_D0_P | 630 | -702.5 |
| 210 | HSSI_D0_N | 690 | -702.5 |
| 211 | HSSI_D0_N | 750 | -702.5 |
| 212 | HSSI_D0_N | 810 | -702.5 |
| 213 | HSSI_D0_N | 870 | -702.5 |
| 214 | VSSAM | 930 | -702.5 |
| 215 | VSSAM | 990 | -702.5 |
| 216 | MVDDL | 1050 | -702.5 |
| 217 | MVDDL | 1110 | -702.5 |
| 218 | MVDDL | 1170 | -702.5 |
| 219 | MVDDA | 1230 | -702.5 |
| 220 | MVDDA | 1290 | -702.5 |
| 221 | MVDDA | 1350 | -702.5 |
| 222 | VDDAM | 1410 | -702.5 |
| 223 | VDDAM | 1470 | -702.5 |
| 224 | VDDAM | 1530 | -702.5 |
| 225 | VDDAM | 1590 | -702.5 |

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| | | | |
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| 226 | VDDAM | 1650 | -702.5 |
| 227 | VDDR | 1710 | -702.5 |
| 228 | VDDR | 1770 | -702.5 |
| 229 | VDDR | 1830 | -702.5 |
| 230 | OSC_TEST | 1890 | -702.5 |
| 231 | TE_R | 1950 | -702.5 |
| 232 | VSSR | 2010 | -702.5 |
| 233 | VSSR | 2070 | -702.5 |
| 234 | VSSR | 2130 | -702.5 |
| 235 | VSSR | 2190 | -702.5 |
| 236 | VREFCP | 2250 | -702.5 |
| 237 | VREFCP | 2310 | -702.5 |
| 238 | VRGH | 2370 | -702.5 |
| 239 | VRGH | 2430 | -702.5 |
| 240 | EXTP | 2490 | -702.5 |
| 241 | EXTP | 2550 | -702.5 |
| 242 | CSP | 2610 | -702.5 |
| 243 | CSP | 2670 | -702.5 |
| 244 | EXTN | 2730 | -702.5 |
| 245 | EXTN | 2790 | -702.5 |
| 246 | CSN | 2850 | -702.5 |
| 247 | CSN | 2910 | -702.5 |
| 248 | VDDB | 2970 | -702.5 |
| 249 | VDDB | 3030 | -702.5 |
| 250 | VDDB | 3090 | -702.5 |
| 251 | VDDB | 3150 | -702.5 |
| 252 | VDDB | 3210 | -702.5 |
| 253 | VDDB | 3270 | -702.5 |
| 254 | VSSB | 3330 | -702.5 |
| 255 | VSSB | 3390 | -702.5 |
| 256 | VSSB | 3450 | -702.5 |
| 257 | VSSB | 3510 | -702.5 |
| 258 | VSSB | 3570 | -702.5 |
| 259 | VSSB | 3630 | -702.5 |
| 260 | C11P | 3690 | -702.5 |
| 261 | C11P | 3750 | -702.5 |
| 262 | C11P | 3810 | -702.5 |
| 263 | C11N | 3870 | -702.5 |
| 264 | C11N | 3930 | -702.5 |
| 265 | C11N | 3990 | -702.5 |
| 266 | C12P | 4050 | -702.5 |
| 267 | C12P | 4110 | -702.5 |
| 268 | C12P | 4170 | -702.5 |
| 269 | C12N | 4230 | -702.5 |
| 270 | C12N | 4290 | -702.5 |
| 271 | C12N | 4350 | -702.5 |
| 272 | C13P | 4410 | -702.5 |
| 273 | C13P | 4470 | -702.5 |
| 274 | C13P | 4530 | -702.5 |
| 275 | C13N | 4590 | -702.5 |
| 276 | C13N | 4650 | -702.5 |
| 277 | C13N | 4710 | -702.5 |
| 278 | C14P | 4770 | -702.5 |
| 279 | C14P | 4830 | -702.5 |
| 280 | C14P | 4890 | -702.5 |
| 281 | C14N | 4950 | -702.5 |
| 282 | C14N | 5010 | -702.5 |
| 283 | C14N | 5070 | -702.5 |
| 284 | AVDD | 5130 | -702.5 |
| 285 | AVDD | 5190 | -702.5 |
| 286 | AVDD | 5250 | -702.5 |
| 287 | AVDD | 5310 | -702.5 |
| 288 | AVSS_AVDD | 5370 | -702.5 |
| 289 | AVSS_AVDD | 5430 | -702.5 |
| 290 | AVSS | 5490 | -702.5 |
| 291 | AVSS | 5550 | -702.5 |
| 292 | AVSS | 5610 | -702.5 |
| 293 | AVEE_AVSS | 5670 | -702.5 |
| 294 | AVEE_AVSS | 5730 | -702.5 |
| 295 | AVEE | 5790 | -702.5 |
| 296 | AVEE | 5850 | -702.5 |
| 297 | AVEE | 5910 | -702.5 |
| 298 | AVEE | 5970 | -702.5 |
| 299 | C21P | 6030 | -702.5 |
| 300 | C21P | 6090 | -702.5 |
| 301 | C21P | 6150 | -702.5 |
| 302 | C21N | 6210 | -702.5 |
| 303 | C21N | 6270 | -702.5 |
| 304 | C21N | 6330 | -702.5 |
| 305 | C22P | 6390 | -702.5 |
| 306 | C22P | 6450 | -702.5 |
| 307 | C22P | 6510 | -702.5 |
| 308 | C22N | 6570 | -702.5 |
| 309 | C22N | 6630 | -702.5 |
| 310 | C22N | 6690 | -702.5 |
| 311 | C23P | 6750 | -702.5 |
| 312 | C23P | 6810 | -702.5 |
| 313 | C23P | 6870 | -702.5 |
| 314 | C23N | 6930 | -702.5 |
| 315 | C23N | 6990 | -702.5 |
| 316 | C23N | 7050 | -702.5 |
| 317 | C24P | 7110 | -702.5 |
| 318 | C24P | 7170 | -702.5 |
| 319 | C24P | 7230 | -702.5 |
| 320 | C24N | 7290 | -702.5 |
| 321 | C24N | 7350 | -702.5 |
| 322 | C24N | 7410 | -702.5 |
| 323 | VDDB | 7470 | -702.5 |
| 324 | VDDB | 7530 | -702.5 |
| 325 | VDDB | 7590 | -702.5 |
| 326 | VDDB | 7650 | -702.5 |
| 327 | VDDB | 7710 | -702.5 |
| 328 | VCL_VDDB | 7770 | -702.5 |
| 329 | VCL_VDDB | 7830 | -702.5 |
| 330 | VCL | 7890 | -702.5 |
| 331 | VCL | 7950 | -702.5 |
| 332 | VCL | 8010 | -702.5 |
| 333 | VCL_AVSS | 8070 | -702.5 |
| 334 | VCL_AVSS | 8130 | -702.5 |
| 335 | AVSS | 8190 | -702.5 |
| 336 | AVSS | 8250 | -702.5 |
| 337 | AVSS | 8310 | -702.5 |
| 338 | VSSB | 8370 | -702.5 |
| 339 | VSSB | 8430 | -702.5 |

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| 340 | VSSB | 8490 | -702.5 |
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| 341 | VSSB | 8550 | -702.5 |
| 342 | C31P | 8610 | -702.5 |
| 343 | C31P | 8670 | -702.5 |
| 344 | C31P | 8730 | -702.5 |
| 345 | C31N | 8790 | -702.5 |
| 346 | C31N | 8850 | -702.5 |
| 347 | C31N | 8910 | -702.5 |
| 348 | C32P | 8970 | -702.5 |
| 349 | C32P | 9030 | -702.5 |
| 350 | C32P | 9090 | -702.5 |
| 351 | C32N | 9150 | -702.5 |
| 352 | C32N | 9210 | -702.5 |
| 353 | C32N | 9270 | -702.5 |
| 354 | DVDD | 9330 | -702.5 |
| 355 | DVDD | 9390 | -702.5 |
| 356 | DVDD | 9450 | -702.5 |
| 357 | DVSS | 9510 | -702.5 |
| 358 | DVSS | 9570 | -702.5 |
| 359 | DVSS | 9630 | -702.5 |
| 360 | C41P | 9690 | -702.5 |
| 361 | C41P | 9750 | -702.5 |
| 362 | C41N | 9810 | -702.5 |
| 363 | C41N | 9870 | -702.5 |
| 364 | VGH | 9930 | -702.5 |
| 365 | VGH | 9990 | -702.5 |
| 366 | VGHO | 10050 | -702.5 |
| 367 | VGHO | 10110 | -702.5 |
| 368 | VRGH | 10170 | -702.5 |
| 369 | VRGH | 10230 | -702.5 |
| 370 | C51P | 10290 | -702.5 |
| 371 | C51P | 10350 | -702.5 |
| 372 | C51N | 10410 | -702.5 |
| 373 | C51N | 10470 | -702.5 |
| 374 | VGL_REG | 10530 | -702.5 |
| 375 | VGL_REG | 10590 | -702.5 |
| 376 | VGLO | 10650 | -702.5 |
| 377 | VGLO | 10710 | -702.5 |
| 378 | VGLX | 10770 | -702.5 |
| 379 | VGLX | 10830 | -702.5 |
| 380 | VGL | 10890 | -702.5 |
| 381 | VGL | 10950 | -702.5 |
| 382 | TEST4 | 11010 | -702.5 |
| 383 | TEST5 | 11070 | -702.5 |
| 384 | TEST6 | 11130 | -702.5 |
| 385 | TEST7 | 11190 | -702.5 |
| 386 | CONTACT2A | 11250 | -702.5 |
| 387 | CONTACT2B | 11310 | -702.5 |
| 388 | VCOM | 11370 | -702.5 |
| 389 | VCOM | 11430 | -702.5 |
| 390 | VCOM | 11490 | -702.5 |
| 391 | VCOM | 11550 | -702.5 |
| 392 | VCOM | 11610 | -702.5 |
| 393 | PADA2 | 11670 | -702.5 |
| 394 | PADB2 | 11730 | -702.5 |
| 395 | VSSIDUM2 | 11790 | -702.5 |
| 396 | VSSIDUM3 | 11880 | -702.5 |
| 397 | VSSIDUM4 | 11760 | 705 |
| 398 | VSSIDUM5 | 11732 | 560 |
| 399 | VSSIDUM6 | 11718 | 705 |
| 400 | PADA3 | 11704 | 560 |
| 401 | PADB3 | 11690 | 705 |
| 402 | VGHO | 11676 | 560 |
| 403 | VGHO | 11662 | 705 |
| 404 | VGHO | 11648 | 560 |
| 405 | VGLO | 11634 | 705 |
| 406 | VGLO | 11620 | 560 |
| 407 | VGLO | 11606 | 705 |
| 408 | GOUT1 | 11592 | 560 |
| 409 | GOUT1 | 11578 | 705 |
| 410 | GOUT2 | 11564 | 560 |
| 411 | GOUT2 | 11550 | 705 |
| 412 | LVGL | 11536 | 560 |
| 413 | LVGL | 11522 | 705 |
| 414 | LVGL | 11508 | 560 |
| 415 | VRGH | 11494 | 705 |
| 416 | VRGH | 11480 | 560 |
| 417 | VRGH | 11466 | 705 |
| 418 | VGLO | 11452 | 560 |
| 419 | VGLO | 11438 | 705 |
| 420 | VGLO | 11424 | 560 |
| 421 | GOUT3 | 11410 | 705 |
| 422 | GOUT3 | 11396 | 560 |
| 423 | GOUT4 | 11382 | 705 |
| 424 | GOUT4 | 11368 | 560 |
| 425 | GOUT5 | 11354 | 705 |
| 426 | GOUT5 | 11340 | 560 |
| 427 | GOUT6 | 11326 | 705 |
| 428 | GOUT6 | 11312 | 560 |
| 429 | GOUT7 | 11298 | 705 |
| 430 | GOUT7 | 11284 | 560 |
| 431 | GOUT8 | 11270 | 705 |
| 432 | GOUT8 | 11256 | 560 |
| 433 | GOUT9 | 11242 | 705 |
| 434 | GOUT9 | 11228 | 560 |
| 435 | GOUT10 | 11214 | 705 |
| 436 | GOUT10 | 11200 | 560 |
| 437 | GOUT11 | 11186 | 705 |
| 438 | GOUT11 | 11172 | 560 |
| 439 | GOUT12 | 11158 | 705 |
| 440 | GOUT12 | 11144 | 560 |
| 441 | GOUT13 | 11130 | 705 |
| 442 | GOUT13 | 11116 | 560 |
| 443 | GOUT14 | 11102 | 705 |
| 444 | GOUT14 | 11088 | 560 |
| 445 | GOUT15 | 11074 | 705 |
| 446 | GOUT15 | 11060 | 560 |
| 447 | GOUT16 | 11046 | 705 |
| 448 | GOUT16 | 11032 | 560 |
| 449 | VGHO | 11018 | 705 |
| 450 | VGHO | 11004 | 560 |
| 451 | VGHO | 10990 | 705 |
| 452 | VGHO | 10976 | 560 |
| 453 | VGHO | 10962 | 705 |

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| 454 | VGHO | 10948 | 560 |
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| 455 | VGHO | 10934 | 705 |
| 456 | VGHO | 10920 | 560 |
| 457 | VGLO | 10906 | 705 |
| 458 | VGLO | 10892 | 560 |
| 459 | VGLO | 10878 | 705 |
| 460 | VGLO | 10864 | 560 |
| 461 | VGLO | 10850 | 705 |
| 462 | VGLO | 10836 | 560 |
| 463 | VGLO | 10822 | 705 |
| 464 | VGLO | 10808 | 560 |
| 465 | VGLO | 10794 | 705 |
| 466 | VSSIDUM7 | 10780 | 560 |
| 467 | VSSIDUM8 | 10766 | 705 |
| 468 | SDUM0 | 10752 | 560 |
| 469 | SDUM1 | 10738 | 705 |
| 470 | S1 | 10724 | 560 |
| 471 | S2 | 10710 | 705 |
| 472 | S3 | 10696 | 560 |
| 473 | S4 | 10682 | 705 |
| 474 | S5 | 10668 | 560 |
| 475 | S6 | 10654 | 705 |
| 476 | S7 | 10640 | 560 |
| 477 | S8 | 10626 | 705 |
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| 479 | S10 | 10598 | 705 |
| 480 | S11 | 10584 | 560 |
| 481 | S12 | 10570 | 705 |
| 482 | S13 | 10556 | 560 |
| 483 | S14 | 10542 | 705 |
| 484 | S15 | 10528 | 560 |
| 485 | S16 | 10514 | 705 |
| 486 | S17 | 10500 | 560 |
| 487 | S18 | 10486 | 705 |
| 488 | S19 | 10472 | 560 |
| 489 | S20 | 10458 | 705 |
| 490 | S21 | 10444 | 560 |
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| 493 | S24 | 10402 | 705 |
| 494 | S25 | 10388 | 560 |
| 495 | S26 | 10374 | 705 |
| 496 | S27 | 10360 | 560 |
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| 499 | S30 | 10318 | 705 |
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| 502 | S33 | 10276 | 560 |
| 503 | S34 | 10262 | 705 |
| 504 | S35 | 10248 | 560 |
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| 506 | S37 | 10220 | 560 |
| 507 | S38 | 10206 | 705 |
| 508 | S39 | 10192 | 560 |
| 509 | S40 | 10178 | 705 |
| 510 | S41 | 10164 | 560 |

| 511 | S42 | 10150 | 705 |
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| 512 | S43 | 10136 | 560 |
| 513 | S44 | 10122 | 705 |
| 514 | S45 | 10108 | 560 |
| 515 | S46 | 10094 | 705 |
| 516 | S47 | 10080 | 560 |
| 517 | S48 | 10066 | 705 |
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| 519 | S50 | 10038 | 705 |
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| 521 | S52 | 10010 | 705 |
| 522 | S53 | 9996 | 560 |
| 523 | S54 | 9982 | 705 |
| 524 | S55 | 9968 | 560 |
| 525 | S56 | 9954 | 705 |
| 526 | S57 | 9940 | 560 |
| 527 | S58 | 9926 | 705 |
| 528 | S59 | 9912 | 560 |
| 529 | S60 | 9898 | 705 |
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| 534 | S65 | 9828 | 560 |
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| 536 | S67 | 9800 | 560 |
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| 538 | S69 | 9772 | 560 |
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| 540 | S71 | 9744 | 560 |
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| 545 | S76 | 9674 | 705 |
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| 548 | S79 | 9632 | 560 |
| 549 | S80 | 9618 | 705 |
| 550 | S81 | 9604 | 560 |
| 551 | S82 | 9590 | 705 |
| 552 | S83 | 9576 | 560 |
| 553 | S84 | 9562 | 705 |
| 554 | S85 | 9548 | 560 |
| 555 | S86 | 9534 | 705 |
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| 558 | S89 | 9492 | 560 |
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| 563 | S94 | 9422 | 705 |
| 564 | S95 | 9408 | 560 |
| 565 | S96 | 9394 | 705 |
| 566 | S97 | 9380 | 560 |
| 567 | S98 | 9366 | 705 |

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| 568 | S99 | 9352 | 560 |
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| 569 | S100 | 9338 | 705 |
| 570 | S101 | 9324 | 560 |
| 571 | S102 | 9310 | 705 |
| 572 | S103 | 9296 | 560 |
| 573 | S104 | 9282 | 705 |
| 574 | S105 | 9268 | 560 |
| 575 | S106 | 9254 | 705 |
| 576 | S107 | 9240 | 560 |
| 577 | S108 | 9226 | 705 |
| 578 | S109 | 9212 | 560 |
| 579 | S110 | 9198 | 705 |
| 580 | S111 | 9184 | 560 |
| 581 | S112 | 9170 | 705 |
| 582 | S113 | 9156 | 560 |
| 583 | S114 | 9142 | 705 |
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| 585 | S116 | 9114 | 705 |
| 586 | S117 | 9100 | 560 |
| 587 | S118 | 9086 | 705 |
| 588 | S119 | 9072 | 560 |
| 589 | S120 | 9058 | 705 |
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| 593 | S124 | 9002 | 705 |
| 594 | S125 | 8988 | 560 |
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| 597 | S128 | 8946 | 705 |
| 598 | S129 | 8932 | 560 |
| 599 | S130 | 8918 | 705 |
| 600 | S131 | 8904 | 560 |
| 601 | S132 | 8890 | 705 |
| 602 | S133 | 8876 | 560 |
| 603 | S134 | 8862 | 705 |
| 604 | S135 | 8848 | 560 |
| 605 | S136 | 8834 | 705 |
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| 610 | S141 | 8764 | 560 |
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| 613 | S144 | 8722 | 705 |
| 614 | S145 | 8708 | 560 |
| 615 | S146 | 8694 | 705 |
| 616 | S147 | 8680 | 560 |
| 617 | S148 | 8666 | 705 |
| 618 | S149 | 8652 | 560 |
| 619 | S150 | 8638 | 705 |
| 620 | S151 | 8624 | 560 |
| 621 | S152 | 8610 | 705 |
| 622 | S153 | 8596 | 560 |
| 623 | S154 | 8582 | 705 |
| 624 | S155 | 8568 | 560 |

| 625 | S156 | 8554 | 705 |
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| 626 | S157 | 8540 | 560 |
| 627 | S158 | 8526 | 705 |
| 628 | S159 | 8512 | 560 |
| 629 | S160 | 8498 | 705 |
| 630 | S161 | 8484 | 560 |
| 631 | S162 | 8470 | 705 |
| 632 | S163 | 8456 | 560 |
| 633 | S164 | 8442 | 705 |
| 634 | S165 | 8428 | 560 |
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| 1179 | S710 | 798 | 705 |
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| 1183 | S714 | 742 | 705 |
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| 1187 | S718 | 686 | 705 |
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| 1192 | VSSIDUM11 | 616 | 560 |
| 1193 | VSSIDUM12 | 602 | 705 |
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| 1195 | VSSIDUM14 | 574 | 705 |
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| 1197 | VSSIDUM16 | 546 | 705 |
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| 1199 | VSSIDUM18 | 518 | 705 |
| 1200 | VSSIDUM19 | 504 | 560 |
| 1201 | VSSIDUM20 | 490 | 705 |
| 1202 | VSSIDUM21 | 476 | 560 |
| 1203 | VSSIDUM22 | 462 | 705 |
| 1204 | VSSIDUM23 | 448 | 560 |
| 1205 | VSSIDUM24 | 434 | 705 |
| 1206 | VSSIDUM25 | 420 | 560 |
| 1207 | VSSIDUM26 | 406 | 705 |
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| 1209 | VSSIDUM28 | 378 | 705 |
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| 1211 | VSSIDUM30 | 350 | 705 |
| 1212 | VSSIDUM31 | 336 | 560 |
| 1213 | VSSIDUM32 | 322 | 705 |
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| 1215 | VSSIDUM34 | 294 | 705 |
| 1216 | VSSIDUM35 | 280 | 560 |
| 1217 | VSSIDUM36 | 266 | 705 |
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| 1219 | VSSIDUM38 | 238 | 705 |
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| 1221 | VSSIDUM40 | 210 | 705 |
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| 1223 | VSSIDUM42 | 182 | 705 |
| 1224 | VSSIDUM43 | 168 | 560 |
| 1225 | VSSIDUM44 | 154 | 705 |
| 1226 | VSSIDUM45 | 140 | 560 |
| 1227 | VSSIDUM46 | 126 | 705 |
| 1228 | VSSIDUM47 | 112 | 560 |
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| 1250 | S732 | -196 | 560 |
| 1251 | S733 | -210 | 705 |

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| 1308 | S790 | -1008 | 560 |

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| 1675 | S1157 | -6146 | 705 |
| 1676 | S1158 | -6160 | 560 |
| 1677 | S1159 | -6174 | 705 |
| 1678 | S1160 | -6188 | 560 |
| 1679 | S1161 | -6202 | 705 |
| 1680 | S1162 | -6216 | 560 |
| 1681 | S1163 | -6230 | 705 |
| 1682 | S1164 | -6244 | 560 |
| 1683 | S1165 | -6258 | 705 |
| 1684 | S1166 | -6272 | 560 |
| 1685 | S1167 | -6286 | 705 |
| 1686 | S1168 | -6300 | 560 |
| 1687 | S1169 | -6314 | 705 |
| 1688 | S1170 | -6328 | 560 |
| 1689 | S1171 | -6342 | 705 |
| 1690 | S1172 | -6356 | 560 |
| 1691 | S1173 | -6370 | 705 |
| 1692 | S1174 | -6384 | 560 |
| 1693 | S1175 | -6398 | 705 |
| 1694 | S1176 | -6412 | 560 |
| 1695 | S1177 | -6426 | 705 |
| 1696 | S1178 | -6440 | 560 |
| 1697 | S1179 | -6454 | 705 |
| 1698 | S1180 | -6468 | 560 |
| 1699 | S1181 | -6482 | 705 |
| 1700 | S1182 | -6496 | 560 |
| 1701 | S1183 | -6510 | 705 |
| 1702 | S1184 | -6524 | 560 |
| 1703 | S1185 | -6538 | 705 |
| 1704 | S1186 | -6552 | 560 |
| 1705 | S1187 | -6566 | 705 |
| 1706 | S1188 | -6580 | 560 |
| 1707 | S1189 | -6594 | 705 |

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| | | | |
|---|---|---|---|
| 1708 | S1190 | -6608 | 560 |
| 1709 | S1191 | -6622 | 705 |
| 1710 | S1192 | -6636 | 560 |
| 1711 | S1193 | -6650 | 705 |
| 1712 | S1194 | -6664 | 560 |
| 1713 | S1195 | -6678 | 705 |
| 1714 | S1196 | -6692 | 560 |
| 1715 | S1197 | -6706 | 705 |
| 1716 | S1198 | -6720 | 560 |
| 1717 | S1199 | -6734 | 705 |
| 1718 | S1200 | -6748 | 560 |
| 1719 | S1201 | -6762 | 705 |
| 1720 | S1202 | -6776 | 560 |
| 1721 | S1203 | -6790 | 705 |
| 1722 | S1204 | -6804 | 560 |
| 1723 | S1205 | -6818 | 705 |
| 1724 | S1206 | -6832 | 560 |
| 1725 | S1207 | -6846 | 705 |
| 1726 | S1208 | -6860 | 560 |
| 1727 | S1209 | -6874 | 705 |
| 1728 | S1210 | -6888 | 560 |
| 1729 | S1211 | -6902 | 705 |
| 1730 | S1212 | -6916 | 560 |
| 1731 | S1213 | -6930 | 705 |
| 1732 | S1214 | -6944 | 560 |
| 1733 | S1215 | -6958 | 705 |
| 1734 | S1216 | -6972 | 560 |
| 1735 | S1217 | -6986 | 705 |
| 1736 | S1218 | -7000 | 560 |
| 1737 | S1219 | -7014 | 705 |
| 1738 | S1220 | -7028 | 560 |
| 1739 | S1221 | -7042 | 705 |
| 1740 | S1222 | -7056 | 560 |
| 1741 | S1223 | -7070 | 705 |
| 1742 | S1224 | -7084 | 560 |
| 1743 | S1225 | -7098 | 705 |
| 1744 | S1226 | -7112 | 560 |
| 1745 | S1227 | -7126 | 705 |
| 1746 | S1228 | -7140 | 560 |
| 1747 | S1229 | -7154 | 705 |
| 1748 | S1230 | -7168 | 560 |
| 1749 | S1231 | -7182 | 705 |
| 1750 | S1232 | -7196 | 560 |
| 1751 | S1233 | -7210 | 705 |
| 1752 | S1234 | -7224 | 560 |
| 1753 | S1235 | -7238 | 705 |
| 1754 | S1236 | -7252 | 560 |
| 1755 | S1237 | -7266 | 705 |
| 1756 | S1238 | -7280 | 560 |
| 1757 | S1239 | -7294 | 705 |
| 1758 | S1240 | -7308 | 560 |
| 1759 | S1241 | -7322 | 705 |
| 1760 | S1242 | -7336 | 560 |
| 1761 | S1243 | -7350 | 705 |
| 1762 | S1244 | -7364 | 560 |
| 1763 | S1245 | -7378 | 705 |
| 1764 | S1246 | -7392 | 560 |
| 1765 | S1247 | -7406 | 705 |
| 1766 | S1248 | -7420 | 560 |
| 1767 | S1249 | -7434 | 705 |
| 1768 | S1250 | -7448 | 560 |
| 1769 | S1251 | -7462 | 705 |
| 1770 | S1252 | -7476 | 560 |
| 1771 | S1253 | -7490 | 705 |
| 1772 | S1254 | -7504 | 560 |
| 1773 | S1255 | -7518 | 705 |
| 1774 | S1256 | -7532 | 560 |
| 1775 | S1257 | -7546 | 705 |
| 1776 | S1258 | -7560 | 560 |
| 1777 | S1259 | -7574 | 705 |
| 1778 | S1260 | -7588 | 560 |
| 1779 | S1261 | -7602 | 705 |
| 1780 | S1262 | -7616 | 560 |
| 1781 | S1263 | -7630 | 705 |
| 1782 | S1264 | -7644 | 560 |
| 1783 | S1265 | -7658 | 705 |
| 1784 | S1266 | -7672 | 560 |
| 1785 | S1267 | -7686 | 705 |
| 1786 | S1268 | -7700 | 560 |
| 1787 | S1269 | -7714 | 705 |
| 1788 | S1270 | -7728 | 560 |
| 1789 | S1271 | -7742 | 705 |
| 1790 | S1272 | -7756 | 560 |
| 1791 | S1273 | -7770 | 705 |
| 1792 | S1274 | -7784 | 560 |
| 1793 | S1275 | -7798 | 705 |
| 1794 | S1276 | -7812 | 560 |
| 1795 | S1277 | -7826 | 705 |
| 1796 | S1278 | -7840 | 560 |
| 1797 | S1279 | -7854 | 705 |
| 1798 | S1280 | -7868 | 560 |
| 1799 | S1281 | -7882 | 705 |
| 1800 | S1282 | -7896 | 560 |
| 1801 | S1283 | -7910 | 705 |
| 1802 | S1284 | -7924 | 560 |
| 1803 | S1285 | -7938 | 705 |
| 1804 | S1286 | -7952 | 560 |
| 1805 | S1287 | -7966 | 705 |
| 1806 | S1288 | -7980 | 560 |
| 1807 | S1289 | -7994 | 705 |
| 1808 | S1290 | -8008 | 560 |
| 1809 | S1291 | -8022 | 705 |
| 1810 | S1292 | -8036 | 560 |
| 1811 | S1293 | -8050 | 705 |
| 1812 | S1294 | -8064 | 560 |
| 1813 | S1295 | -8078 | 705 |
| 1814 | S1296 | -8092 | 560 |
| 1815 | S1297 | -8106 | 705 |
| 1816 | S1298 | -8120 | 560 |
| 1817 | S1299 | -8134 | 705 |
| 1818 | S1300 | -8148 | 560 |
| 1819 | S1301 | -8162 | 705 |
| 1820 | S1302 | -8176 | 560 |
| 1821 | S1303 | -8190 | 705 |

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| | | | |
|---|---|---|---|
| 1822 | S1304 | -8204 | 560 |
| 1823 | S1305 | -8218 | 705 |
| 1824 | S1306 | -8232 | 560 |
| 1825 | S1307 | -8246 | 705 |
| 1826 | S1308 | -8260 | 560 |
| 1827 | S1309 | -8274 | 705 |
| 1828 | S1310 | -8288 | 560 |
| 1829 | S1311 | -8302 | 705 |
| 1830 | S1312 | -8316 | 560 |
| 1831 | S1313 | -8330 | 705 |
| 1832 | S1314 | -8344 | 560 |
| 1833 | S1315 | -8358 | 705 |
| 1834 | S1316 | -8372 | 560 |
| 1835 | S1317 | -8386 | 705 |
| 1836 | S1318 | -8400 | 560 |
| 1837 | S1319 | -8414 | 705 |
| 1838 | S1320 | -8428 | 560 |
| 1839 | S1321 | -8442 | 705 |
| 1840 | S1322 | -8456 | 560 |
| 1841 | S1323 | -8470 | 705 |
| 1842 | S1324 | -8484 | 560 |
| 1843 | S1325 | -8498 | 705 |
| 1844 | S1326 | -8512 | 560 |
| 1845 | S1327 | -8526 | 705 |
| 1846 | S1328 | -8540 | 560 |
| 1847 | S1329 | -8554 | 705 |
| 1848 | S1330 | -8568 | 560 |
| 1849 | S1331 | -8582 | 705 |
| 1850 | S1332 | -8596 | 560 |
| 1851 | S1333 | -8610 | 705 |
| 1852 | S1334 | -8624 | 560 |
| 1853 | S1335 | -8638 | 705 |
| 1854 | S1336 | -8652 | 560 |
| 1855 | S1337 | -8666 | 705 |
| 1856 | S1338 | -8680 | 560 |
| 1857 | S1339 | -8694 | 705 |
| 1858 | S1340 | -8708 | 560 |
| 1859 | S1341 | -8722 | 705 |
| 1860 | S1342 | -8736 | 560 |
| 1861 | S1343 | -8750 | 705 |
| 1862 | S1344 | -8764 | 560 |
| 1863 | S1345 | -8778 | 705 |
| 1864 | S1346 | -8792 | 560 |
| 1865 | S1347 | -8806 | 705 |
| 1866 | S1348 | -8820 | 560 |
| 1867 | S1349 | -8834 | 705 |
| 1868 | S1350 | -8848 | 560 |
| 1869 | S1351 | -8862 | 705 |
| 1870 | S1352 | -8876 | 560 |
| 1871 | S1353 | -8890 | 705 |
| 1872 | S1354 | -8904 | 560 |
| 1873 | S1355 | -8918 | 705 |
| 1874 | S1356 | -8932 | 560 |
| 1875 | S1357 | -8946 | 705 |
| 1876 | S1358 | -8960 | 560 |
| 1877 | S1359 | -8974 | 705 |
| 1878 | S1360 | -8988 | 560 |
| 1879 | S1361 | -9002 | 705 |
| 1880 | S1362 | -9016 | 560 |
| 1881 | S1363 | -9030 | 705 |
| 1882 | S1364 | -9044 | 560 |
| 1883 | S1365 | -9058 | 705 |
| 1884 | S1366 | -9072 | 560 |
| 1885 | S1367 | -9086 | 705 |
| 1886 | S1368 | -9100 | 560 |
| 1887 | S1369 | -9114 | 705 |
| 1888 | S1370 | -9128 | 560 |
| 1889 | S1371 | -9142 | 705 |
| 1890 | S1372 | -9156 | 560 |
| 1891 | S1373 | -9170 | 705 |
| 1892 | S1374 | -9184 | 560 |
| 1893 | S1375 | -9198 | 705 |
| 1894 | S1376 | -9212 | 560 |
| 1895 | S1377 | -9226 | 705 |
| 1896 | S1378 | -9240 | 560 |
| 1897 | S1379 | -9254 | 705 |
| 1898 | S1380 | -9268 | 560 |
| 1899 | S1381 | -9282 | 705 |
| 1900 | S1382 | -9296 | 560 |
| 1901 | S1383 | -9310 | 705 |
| 1902 | S1384 | -9324 | 560 |
| 1903 | S1385 | -9338 | 705 |
| 1904 | S1386 | -9352 | 560 |
| 1905 | S1387 | -9366 | 705 |
| 1906 | S1388 | -9380 | 560 |
| 1907 | S1389 | -9394 | 705 |
| 1908 | S1390 | -9408 | 560 |
| 1909 | S1391 | -9422 | 705 |
| 1910 | S1392 | -9436 | 560 |
| 1911 | S1393 | -9450 | 705 |
| 1912 | S1394 | -9464 | 560 |
| 1913 | S1395 | -9478 | 705 |
| 1914 | S1396 | -9492 | 560 |
| 1915 | S1397 | -9506 | 705 |
| 1916 | S1398 | -9520 | 560 |
| 1917 | S1399 | -9534 | 705 |
| 1918 | S1400 | -9548 | 560 |
| 1919 | S1401 | -9562 | 705 |
| 1920 | S1402 | -9576 | 560 |
| 1921 | S1403 | -9590 | 705 |
| 1922 | S1404 | -9604 | 560 |
| 1923 | S1405 | -9618 | 705 |
| 1924 | S1406 | -9632 | 560 |
| 1925 | S1407 | -9646 | 705 |
| 1926 | S1408 | -9660 | 560 |
| 1927 | S1409 | -9674 | 705 |
| 1928 | S1410 | -9688 | 560 |
| 1929 | S1411 | -9702 | 705 |
| 1930 | S1412 | -9716 | 560 |
| 1931 | S1413 | -9730 | 705 |
| 1932 | S1414 | -9744 | 560 |
| 1933 | S1415 | -9758 | 705 |
| 1934 | S1416 | -9772 | 560 |
| 1935 | S1417 | -9786 | 705 |

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| | | | |
|---|---|---|---|
| 1936 | S1418 | -9800 | 560 |
| 1937 | S1419 | -9814 | 705 |
| 1938 | S1420 | -9828 | 560 |
| 1939 | S1421 | -9842 | 705 |
| 1940 | S1422 | -9856 | 560 |
| 1941 | S1423 | -9870 | 705 |
| 1942 | S1424 | -9884 | 560 |
| 1943 | S1425 | -9898 | 705 |
| 1944 | S1426 | -9912 | 560 |
| 1945 | S1427 | -9926 | 705 |
| 1946 | S1428 | -9940 | 560 |
| 1947 | S1429 | -9954 | 705 |
| 1948 | S1430 | -9968 | 560 |
| 1949 | S1431 | -9982 | 705 |
| 1950 | S1432 | -9996 | 560 |
| 1951 | S1433 | -10010 | 705 |
| 1952 | S1434 | -10024 | 560 |
| 1953 | S1435 | -10038 | 705 |
| 1954 | S1436 | -10052 | 560 |
| 1955 | S1437 | -10066 | 705 |
| 1956 | S1438 | -10080 | 560 |
| 1957 | S1439 | -10094 | 705 |
| 1958 | S1440 | -10108 | 560 |
| 1959 | SDUM2 | -10122 | 705 |
| 1960 | SDUM3 | -10136 | 560 |
| 1961 | VSSIDUM58 | -10150 | 705 |
| 1962 | VSSIDUM59 | -10164 | 560 |
| 1963 | VGLO | -10178 | 705 |
| 1964 | VGLO | -10192 | 560 |
| 1965 | VGLO | -10206 | 705 |
| 1966 | VGLO | -10220 | 560 |
| 1967 | VGLO | -10234 | 705 |
| 1968 | VGLO | -10248 | 560 |
| 1969 | VGLO | -10262 | 705 |
| 1970 | VGLO | -10276 | 560 |
| 1971 | VGLO | -10290 | 705 |
| 1972 | VGHO | -10304 | 560 |
| 1973 | VGHO | -10318 | 705 |
| 1974 | VGHO | -10332 | 560 |
| 1975 | VGHO | -10346 | 705 |
| 1976 | VGHO | -10360 | 560 |
| 1977 | VGHO | -10374 | 705 |
| 1978 | VGHO | -10388 | 560 |
| 1979 | VGHO | -10402 | 705 |
| 1980 | VSSIDUM60 | -10416 | 560 |
| 1981 | VSSIDUM61 | -10430 | 705 |
| 1982 | VSSIDUM62 | -10444 | 560 |
| 1983 | VSSIDUM63 | -10458 | 705 |
| 1984 | VSSIDUM64 | -10472 | 560 |
| 1985 | VSSIDUM65 | -10486 | 705 |
| 1986 | VSSIDUM66 | -10500 | 560 |
| 1987 | VSSIDUM67 | -10514 | 705 |
| 1988 | VSSIDUM68 | -10528 | 560 |
| 1989 | VSSIDUM69 | -10542 | 705 |
| 1990 | VSSIDUM70 | -10556 | 560 |
| 1991 | VSSIDUM71 | -10570 | 705 |
| 1992 | VSSIDUM72 | -10584 | 560 |
| 1993 | VSSIDUM73 | -10598 | 705 |
| 1994 | VSSIDUM74 | -10612 | 560 |
| 1995 | VSSIDUM75 | -10626 | 705 |
| 1996 | VSSIDUM76 | -10640 | 560 |
| 1997 | VSSIDUM77 | -10654 | 705 |
| 1998 | VSSIDUM78 | -10668 | 560 |
| 1999 | VSSIDUM79 | -10682 | 705 |
| 2000 | VSSIDUM80 | -10696 | 560 |
| 2001 | VSSIDUM81 | -10710 | 705 |
| 2002 | VSSIDUM82 | -10724 | 560 |
| 2003 | VSSIDUM83 | -10738 | 705 |
| 2004 | VSSIDUM84 | -10752 | 560 |
| 2005 | VSSIDUM85 | -10766 | 705 |
| 2006 | VSSIDUM86 | -10780 | 560 |
| 2007 | VSSIDUM87 | -10794 | 705 |
| 2008 | VSSIDUM88 | -10808 | 560 |
| 2009 | VSSIDUM89 | -10822 | 705 |
| 2010 | VSSIDUM90 | -10836 | 560 |
| 2011 | VSSIDUM91 | -10850 | 705 |
| 2012 | VSSIDUM92 | -10864 | 560 |
| 2013 | VSSIDUM93 | -10878 | 705 |
| 2014 | VSSIDUM94 | -10892 | 560 |
| 2015 | VSSIDUM95 | -10906 | 705 |
| 2016 | VSSIDUM96 | -10920 | 560 |
| 2017 | VSSIDUM97 | -10934 | 705 |
| 2018 | VSSIDUM98 | -10948 | 560 |
| 2019 | VSSIDUM99 | -10962 | 705 |
| 2020 | VSSIDUM100 | -10976 | 560 |
| 2021 | VSSIDUM101 | -10990 | 705 |
| 2022 | VSSIDUM102 | -11004 | 560 |
| 2023 | VSSIDUM103 | -11018 | 705 |
| 2024 | GOUT17 | -11032 | 560 |
| 2025 | GOUT17 | -11046 | 705 |
| 2026 | GOUT18 | -11060 | 560 |
| 2027 | GOUT18 | -11074 | 705 |
| 2028 | GOUT19 | -11088 | 560 |
| 2029 | GOUT19 | -11102 | 705 |
| 2030 | GOUT20 | -11116 | 560 |
| 2031 | GOUT20 | -11130 | 705 |
| 2032 | GOUT21 | -11144 | 560 |
| 2033 | GOUT21 | -11158 | 705 |
| 2034 | GOUT22 | -11172 | 560 |
| 2035 | GOUT22 | -11186 | 705 |
| 2036 | GOUT23 | -11200 | 560 |
| 2037 | GOUT23 | -11214 | 705 |
| 2038 | GOUT24 | -11228 | 560 |
| 2039 | GOUT24 | -11242 | 705 |
| 2040 | GOUT25 | -11256 | 560 |
| 2041 | GOUT25 | -11270 | 705 |
| 2042 | GOUT26 | -11284 | 560 |
| 2043 | GOUT26 | -11298 | 705 |
| 2044 | GOUT27 | -11312 | 560 |
| 2045 | GOUT27 | -11326 | 705 |
| 2046 | GOUT28 | -11340 | 560 |
| 2047 | GOUT28 | -11354 | 705 |
| 2048 | GOUT29 | -11368 | 560 |
| 2049 | GOUT29 | -11382 | 705 |

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| | | | |
|---|---|---|---|
| 2050 | GOUT30 | -11396 | 560 |
| 2051 | GOUT30 | -11410 | 705 |
| 2052 | VGLO | -11424 | 560 |
| 2053 | VGLO | -11438 | 705 |
| 2054 | VGLO | -11452 | 560 |
| 2055 | VRGH | -11466 | 705 |
| 2056 | VRGH | -11480 | 560 |
| 2057 | VRGH | -11494 | 705 |
| 2058 | LVGL | -11508 | 560 |
| 2059 | LVGL | -11522 | 705 |
| 2060 | LVGL | -11536 | 560 |
| 2061 | GOUT31 | -11550 | 705 |
| 2062 | GOUT31 | -11564 | 560 |
| 2063 | GOUT32 | -11578 | 705 |
| 2064 | GOUT32 | -11592 | 560 |
| 2065 | VGLO | -11606 | 705 |
| 2066 | VGLO | -11620 | 560 |
| 2067 | VGLO | -11634 | 705 |
| 2068 | VGHO | -11648 | 560 |
| 2069 | VGHO | -11662 | 705 |
| 2070 | VGHO | -11676 | 560 |
| 2071 | PADA4 | -11690 | 705 |
| 2072 | PADB4 | -11704 | 560 |
| 2073 | VSSIDUM104 | -11718 | 705 |
| 2074 | VSSIDUM105 | -11732 | 560 |
| 2075 | VSSIDUM106 | -11760 | 705 |

| | | |
|---|---|---|
| Alighmark LEFT | -11870 | 687.5 |
| Alignmark RIGHT | 11870 | 687.5 |

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# 6. Block Function Description

**Interface**

The RM68120 incorporates command method 24-/16-/8-bits bus display command interface. WDR stores data to be written into GRAM or parameters temporarily while RDR stores data read out from GRAM temporarily. When data is written from microcomputer to GRAM, the RM68120 writes firstly to WDR, and then the data is written to GRAM automatically by internal operation. Because read out operation from GRAM is conducted through RDR, first read out data is invalid. Normal data is read out from 2nd read out data.

**Address Counter (AC)**

Address counter (AC) gives address to GRAM. When command setting address is written to CR, the data is transferred from CR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or –1 automatically. AC after data is read out increments by +1 or –1 likewise. The RM68120 writes data to only rectangular area that was specified by GRAM.

**Graphic RAM (GRAM)**

The graphic RAM (GRAM) stores 1,244,160 bytes pattern data using 24 bits for one pixel, enabling maximum 480RGB x 864 dot graphic display.

**Grayscale Voltage Generating Circuit**

Grayscale voltage generating circuit generates an TFT-LCD drive voltage, which corresponds to grayscale level set in the γ correction register. The RM68120 displays 16.7M colors at the maximum.

**Power Supply Circuit**

The power supply circuit generates supply voltages to TFT-LCD panel, VREG1OUT, VGH, and VGL.

**Timing Generating**

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

**Oscillator**

The RM68120 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

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**Panel Driver Circuit**

The TFT-LCD display driver circuit consists of 1440 source drivers (S1~S1440). Display pattern data is latched when 1440 data is input. This latched data controls source drivers and outputs drive waveform. The shift direction of 1440-dot output from the source driver can be changed by setting commands. The gate signal consists from GOUT1 to GOUT32 and outputs either VGHR or VGLR level.

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# 7. Function Description

### 7.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show below.

| IM[3:0] | Display Data | Command |
|---|---|---|
| 0000 | 80-series 8-bit MPU I/F, D[7:0] | 80-series 8-bit MPU I/F, D[7:0] |
| 0001 | 80-series 16-bit MPU I/F, D[15:0] | 80-series 16-bit MPU I/F, D[15:0] |
| 0010 | 80-series 24-bit MPU I/F, D[23:0] | 80-series 24-bit MPU I/F, D[23:0] |
| 0011 | RGB I/F, D[23:0] | 16-bit SPI (SCL rising edge trigger), SDI/SDO |
| 0100 | RGB I/F, D[23:0] | I2C I/F, I2C_SDA |
| 0101 | MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N | MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N |
| 1101 | MIPI DSI,HSSI_D0_P/N, HSSI_D1_P/N | MIPI DSI,HSSI_D0_P/N,HSSI_D1_P/N (Video Mode) |
| 0110 | MDDI,HSSI_D0_P/N, HSSI_D1_P/N | MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>16-bit SPI (SCL rising edge trigger), SDI/SDO |
| 1110 | MDDI,HSSI_D0_P/N, HSSI_D1_P/N | MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>16-bit SPI (SCL falling edge trigger), SDI/SDO |
| 0111 | MDDI,HSSI_D0_P/N, HSSI_D1_P/N | MDDI, HSSI_D0_P/N, HSSI_D1_P/N<br>I2C I/F, I2C_SDA serial data |
| 1011 | RGB I/F, D[23:0] | 16-bit SPI (SCL falling edge trigger), SDI/SDO |

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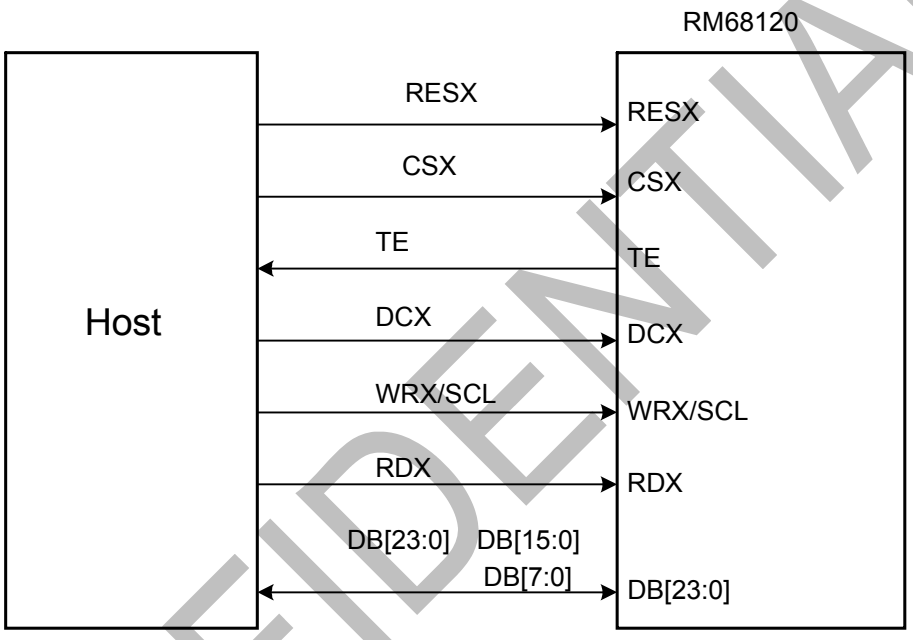
### 7.2 Display Bus Interface (DBI)

The RM68120 uses a 28-wires 24-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and DB[23:0] is parallel DBI data. There are three 24/16/8-bit types interface supported for the display data transfer. The graphics controller chip reads the data at the rising edge of RDX signal. The DCX is data/command flag. When DCX = "1", D23 to D0 bits are display RAM data or command parameters. When DCX = "0", D7 to D0 bits are commands.

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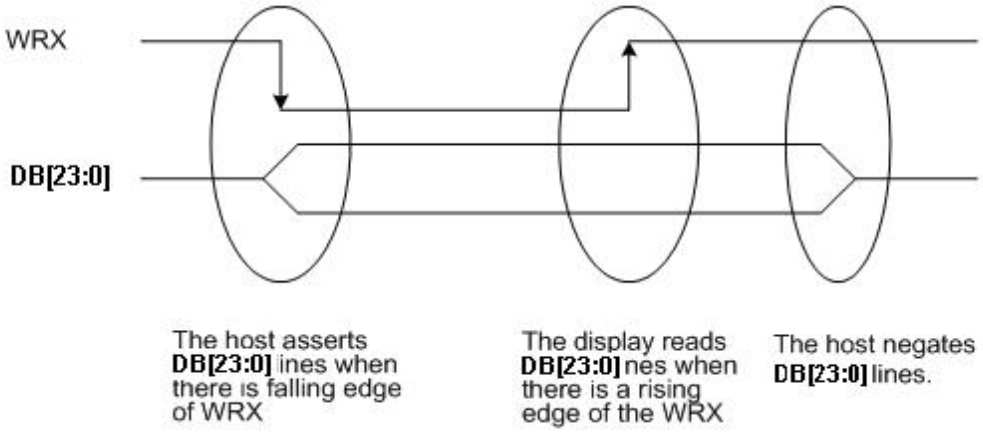
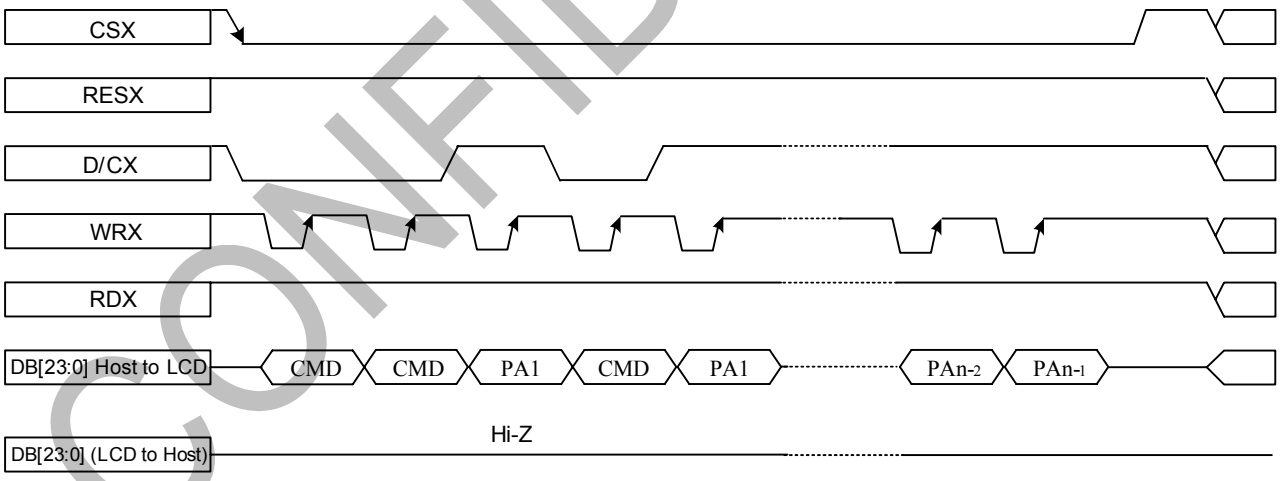
### 7.2.1 Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (DB[23:0]). WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. DCX is driven low while command information is on the interface and is pulled high when data is present.

The following figure shows a write cycle for the type B interface.

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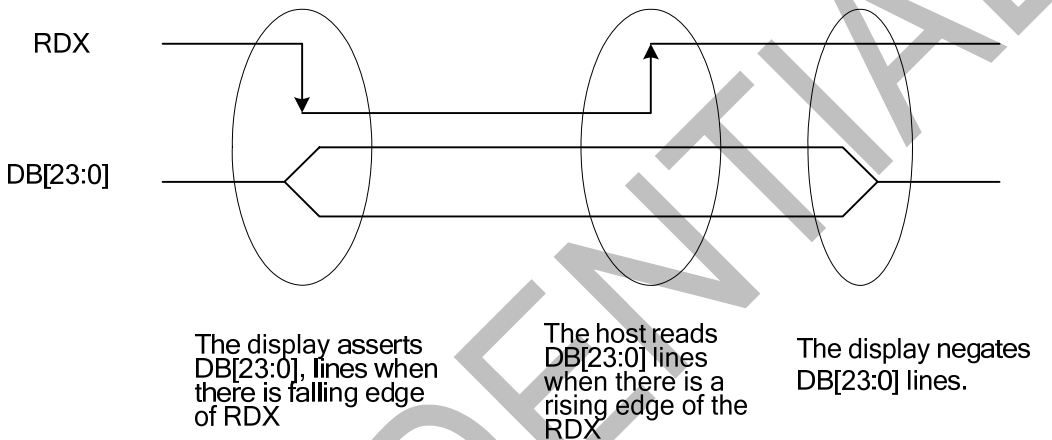
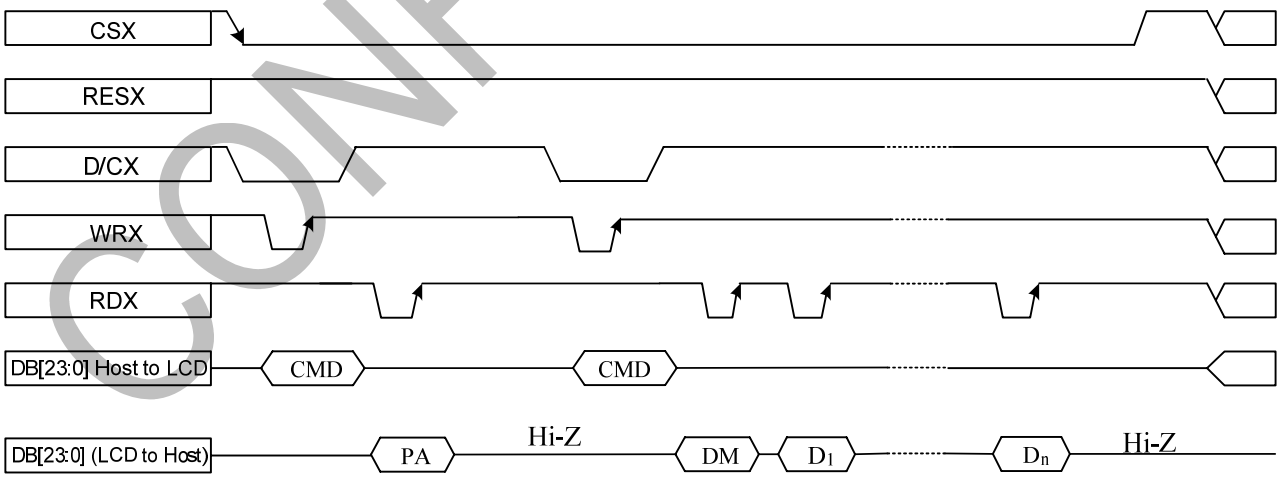
### 7.2.2 Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (D[23:0]). RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. DCX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.




Note: RDX is an unsynchronized signal (It can be stopped).




Note: Read Data is only valid when the DCX input is pulled high. If DCX is driven low during read then the display information outputs will be High-Z.

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DBI Type B Interface

24-bit data bus DB[23:0] interface, IM[3:0] = 0010
IFPF[3:0]: command_3A[3:0]

| | IFPF | DB 23 | DB 22 | DB 21 | DB 20 | DB 19 | DB 18 | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command Write | * | | | | | | | | | | | | | | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| Command Read | * | | | | | | | | | | | | | | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |

| | IFPF | DB 23 | DB 22 | DB 21 | DB 20 | DB 19 | DB 18 | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Memory Write | 5 | | | | | | | | | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0] | 65K |
| | 6 | | | | | | | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | 262K |
| | 7 | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | 16.7M |

The read data for RGB is 24 bit output as below.

| | DB 23 | DB 22 | DB 21 | DB 20 | DB 19 | DB 18 | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Memory Read | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | 16.7M |

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16-bit data bus DB[15:0] interface, IM[3:0] = 0001

| | IFPF | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command Write | * | | | | | | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| Command Read | * | | | | | | | | | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |

| | IFPF | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Memory Write | 5 | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0] | 65K |
| | 6 | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | X | X | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | X | X | 262K |
| | | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | X | X | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | X | X | |
| | | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | X | X | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | X | X | |
| | 7 | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | 16.7M |
| | | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | |
| | | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | |

The read data for RGB is 16 bit output as below.

| | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Memory Read | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | 16.7M |
| | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | | | | | | | | | |

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8-bit data bus DB[7:0] interface, IM[3:0] = 0000

| | IFPF | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 |
|---|---|---|---|---|---|---|---|---|---|
| Command Write | * | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| Command Read | * | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |

| | IFPF | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|
| Memory Write | 5 | R[4] | R[3] | R[2] | R[1] | R[0] | G[5] | G[4] | G[3] | 65K |
| | | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0] | |
| | 6 | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | X | X | 262K |
| | | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | X | X | |
| | | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | X | X | |
| | 7 | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | 16.7M |
| | | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | |
| | | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | |

The read data for RGB is 8 bit output as below.

| | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|
| Memory Read | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | 16.7M |
| | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | |
| | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | |

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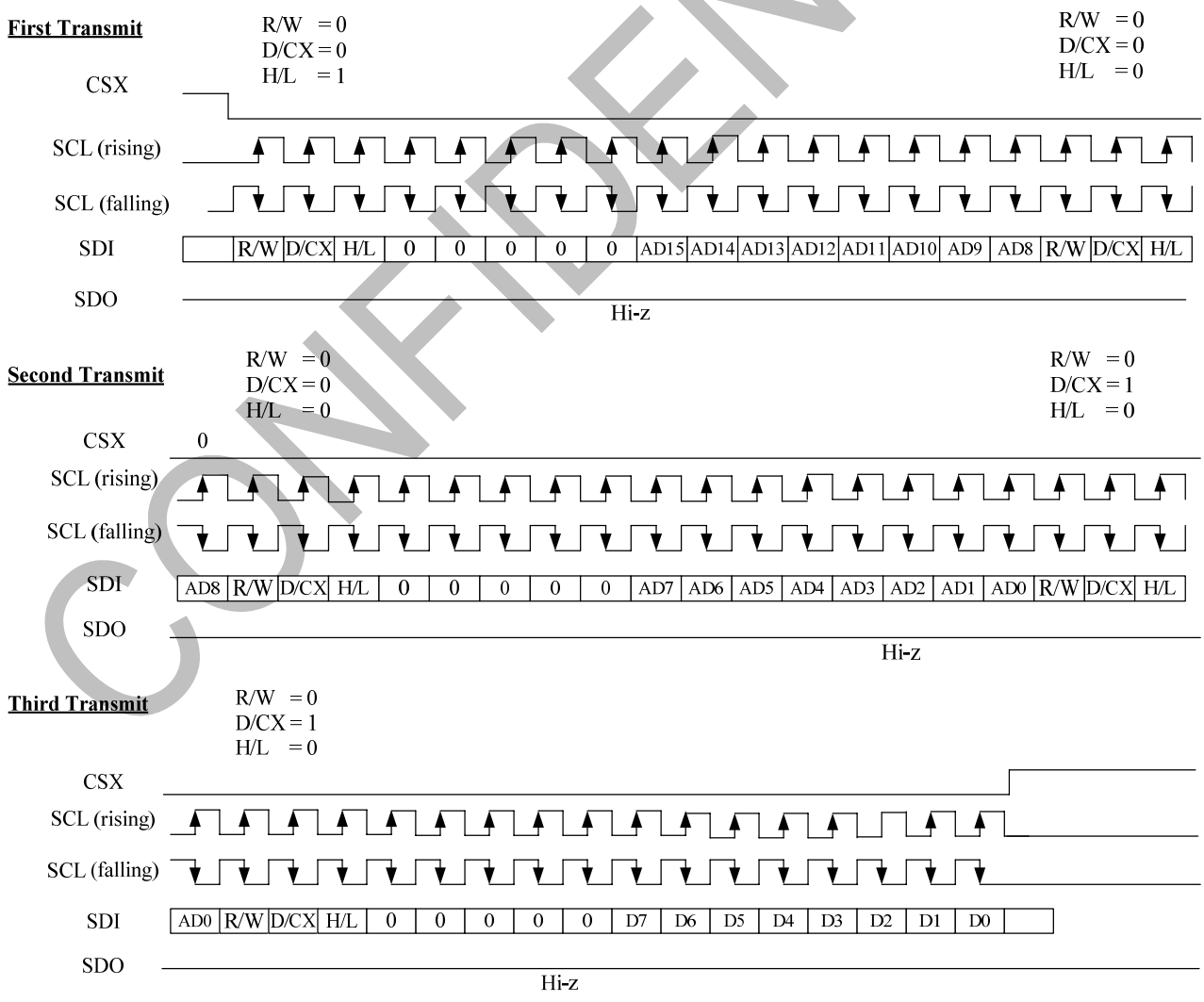
### 7.3 Serial Interface

#### 7.3.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface write command sequences are described in the following figure.

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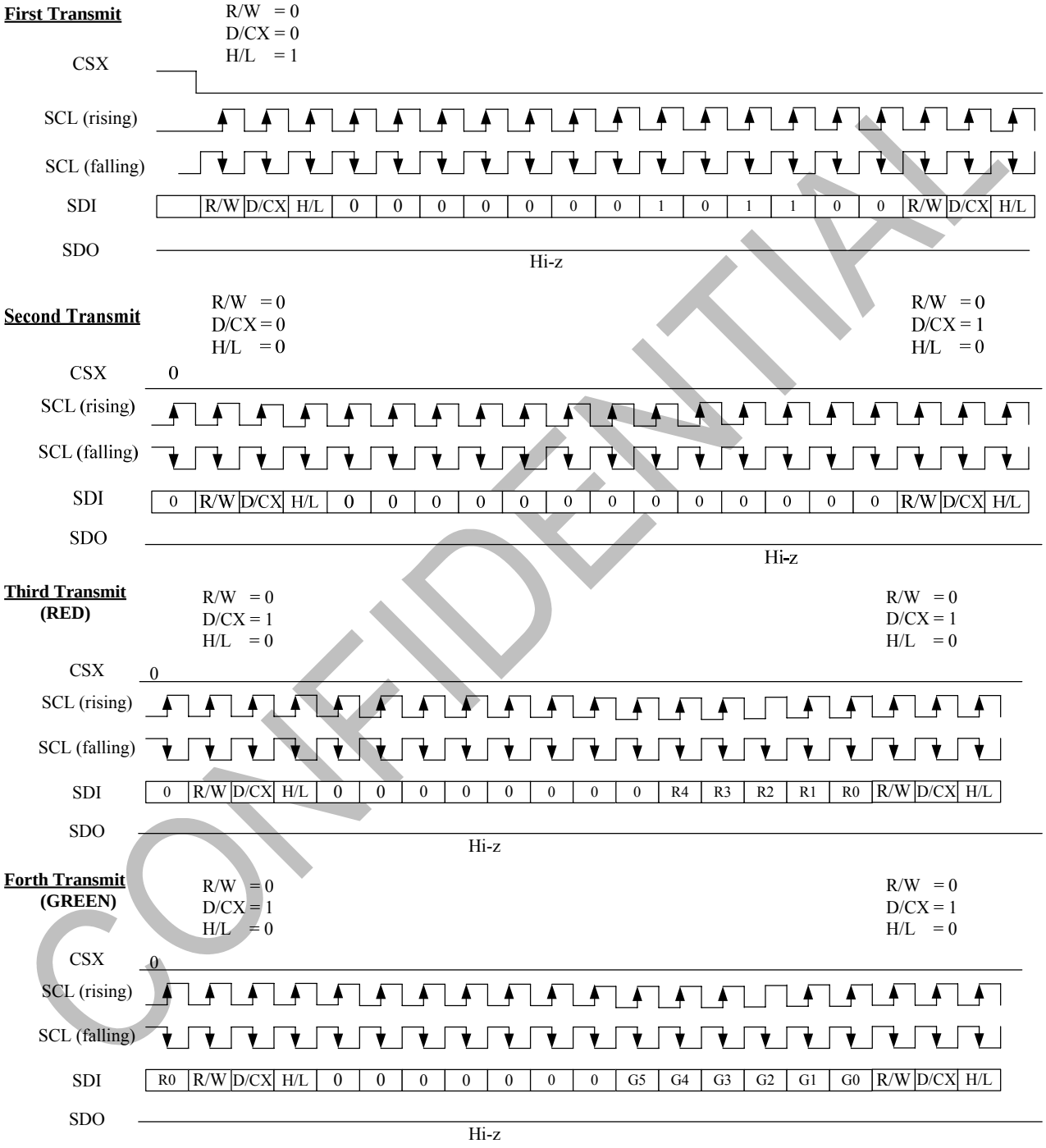
The SPI interface write data sequences are described in the following figure.

SRAM write: 65K colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)

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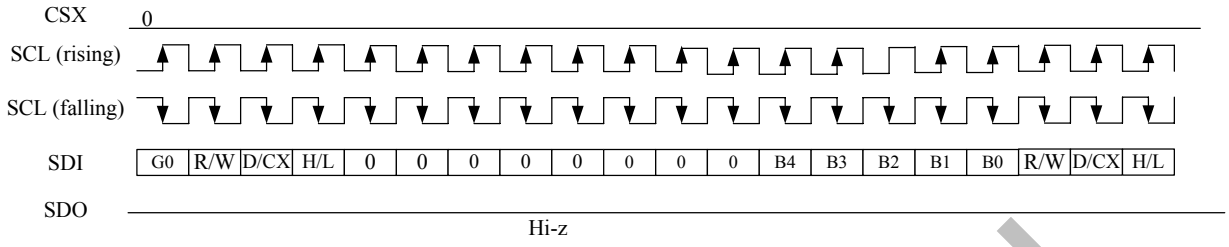
**Fifth Transmit**
**(BLUE)**

R/W = 0
D/CX = 1
H/L = 0

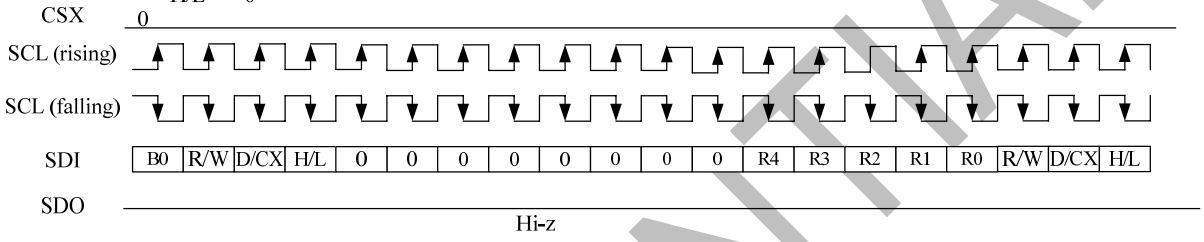
R/W = 0
D/CX = 1
H/L = 0




**Sixth Transmit**
**(RED)**

R/W = 0
D/CX = 1
H/L = 0

R/W = 0
D/CX = 1
H/L = 0

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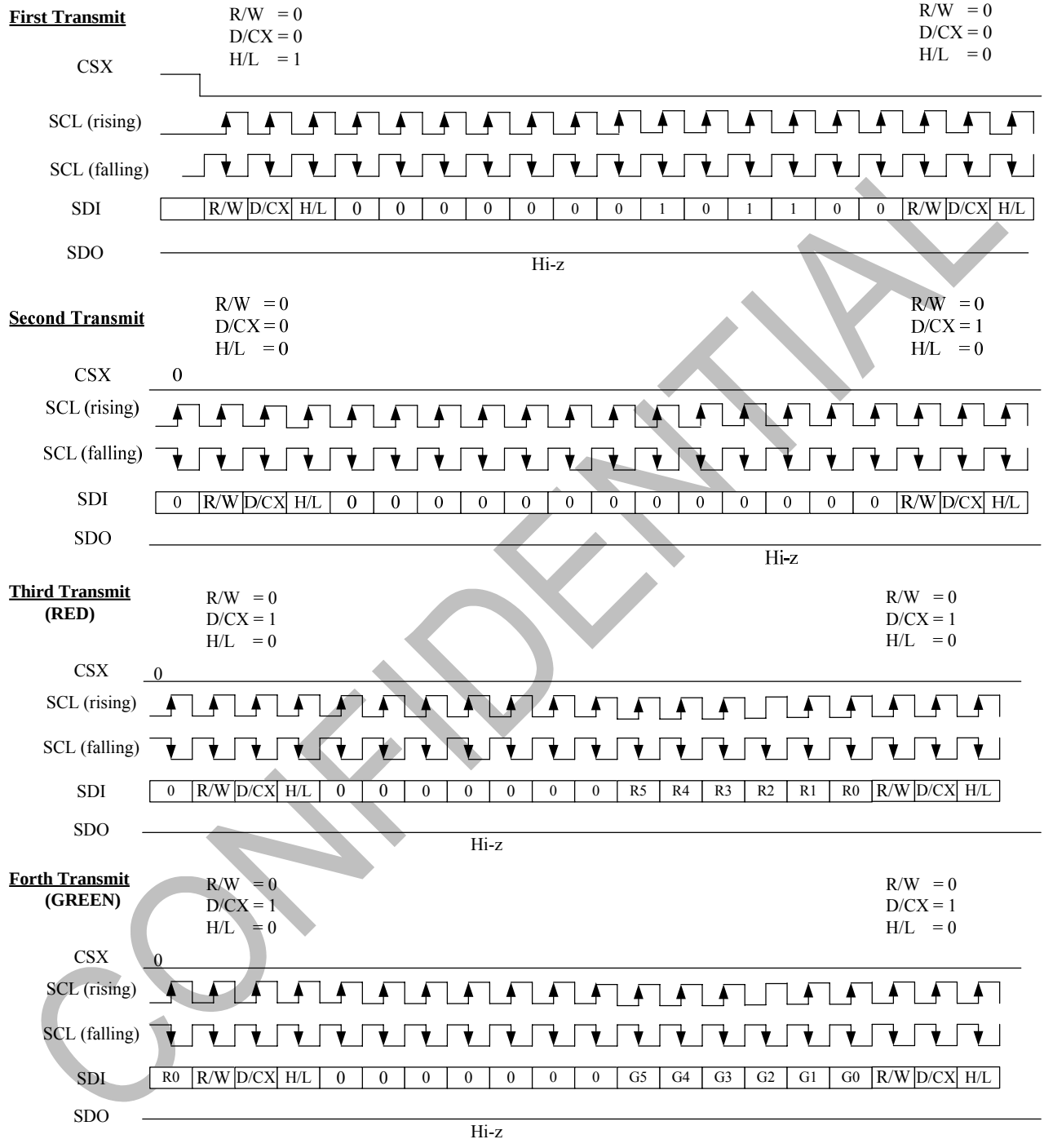
SRAM write: 262K colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)

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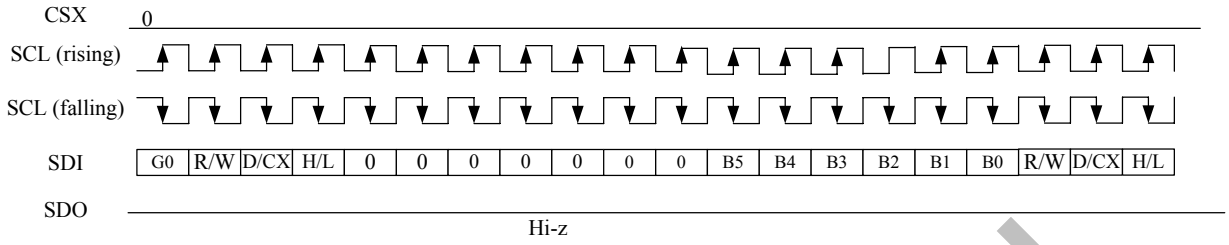
**Fifth Transmit**
**(BLUE)**

R/W = 0
D/CX = 1
H/L = 0

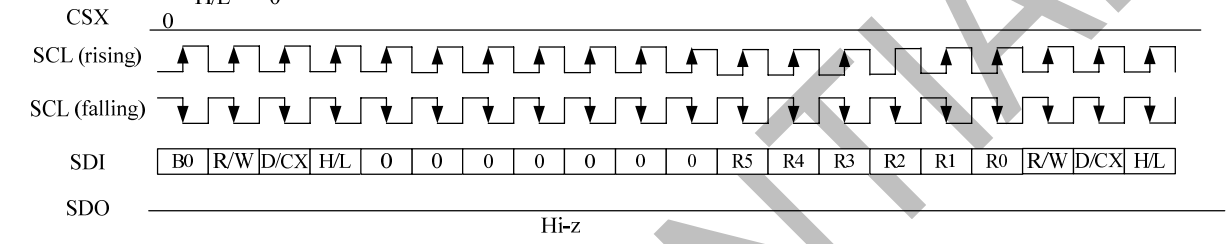
R/W = 0
D/CX = 1
H/L = 0




**Sixth Transmit**
**(RED)**

R/W = 0
D/CX = 1
H/L = 0

R/W = 0
D/CX = 1
H/L = 0

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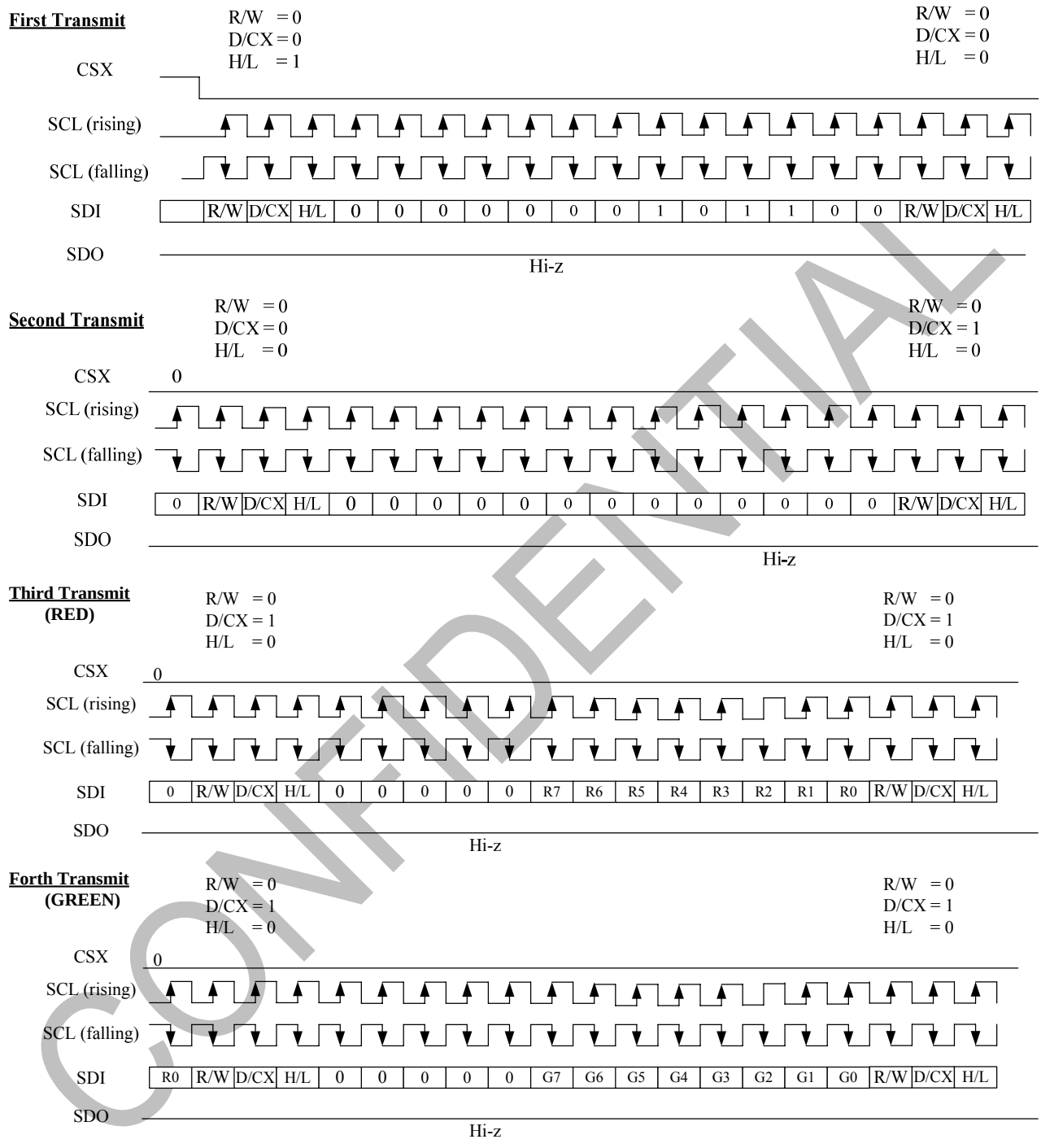
SRAM write: 16.7K colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)

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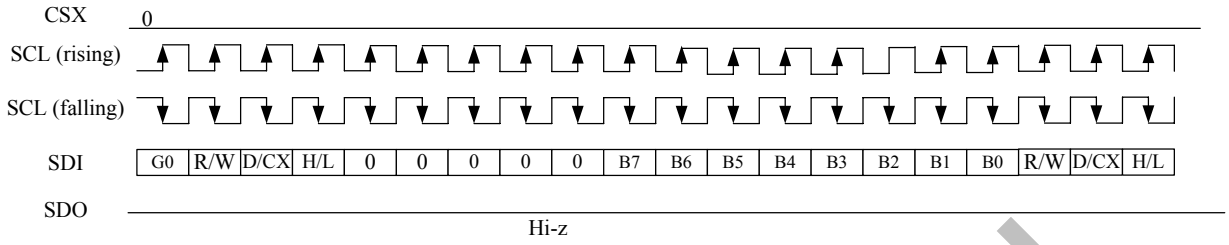
**Fifth Transmit**
**(BLUE)**

R/W = 0
D/CX = 1
H/L = 0

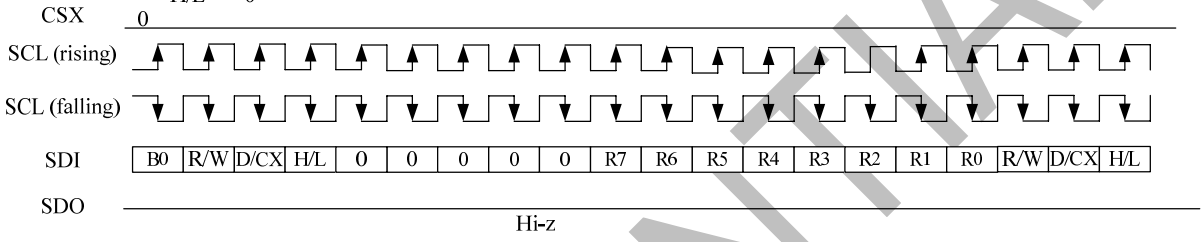
R/W = 0
D/CX = 1
H/L = 0




**Sixth Transmit**
**(RED)**

R/W = 0
D/CX = 1
H/L = 0

R/W = 0
D/CX = 1
H/L = 0

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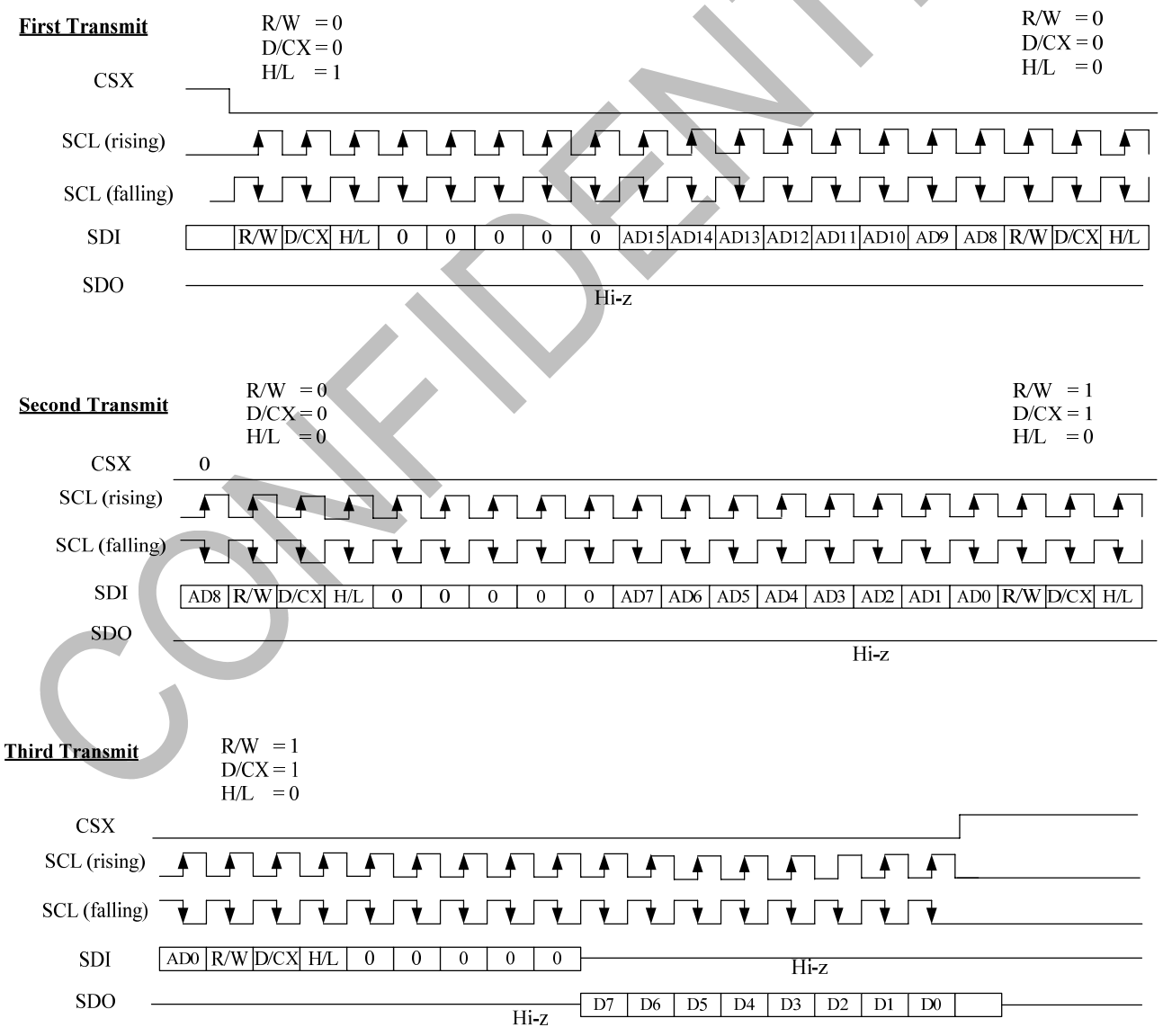
### 7.3.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface read command sequences are described in the following figure.

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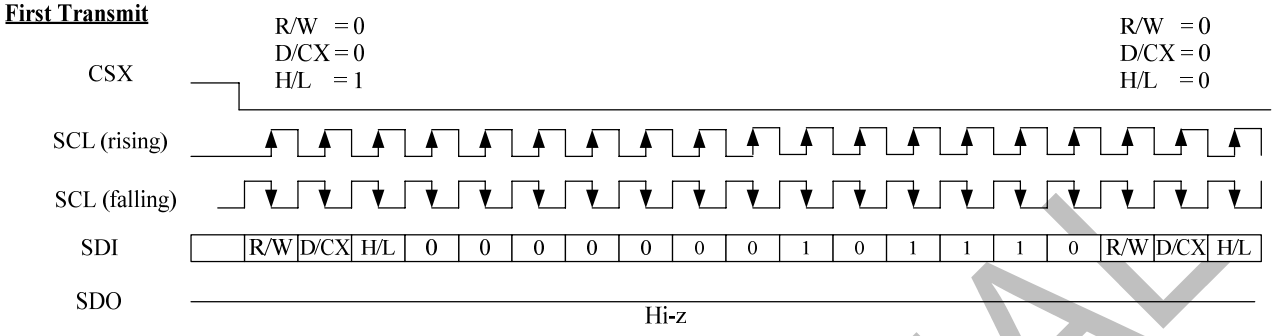
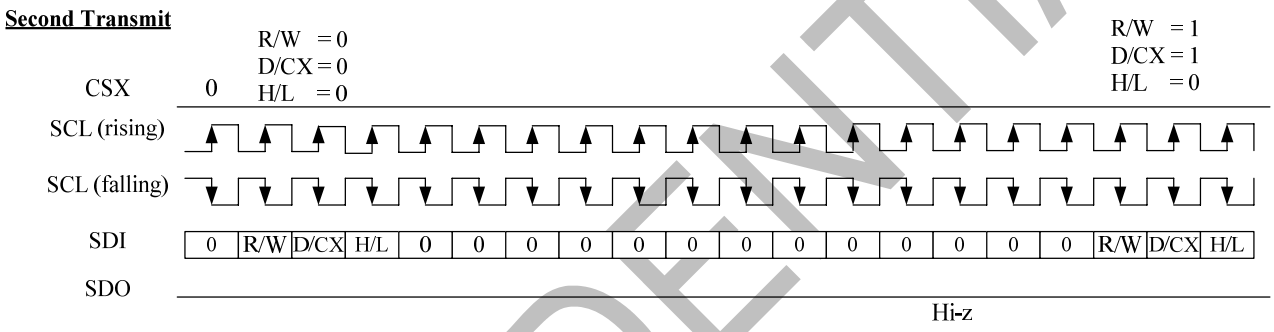
The SPI interface read data sequences are described in the following figure.

SRAM read: 65K colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)

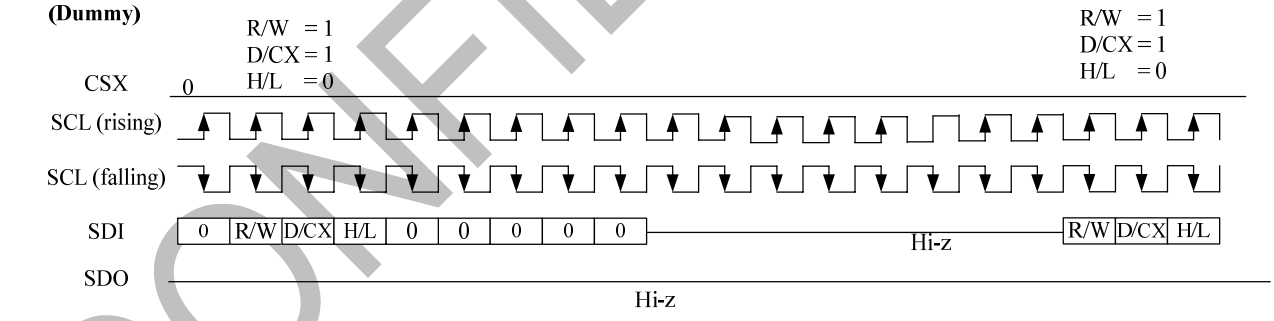
**First Transmit**



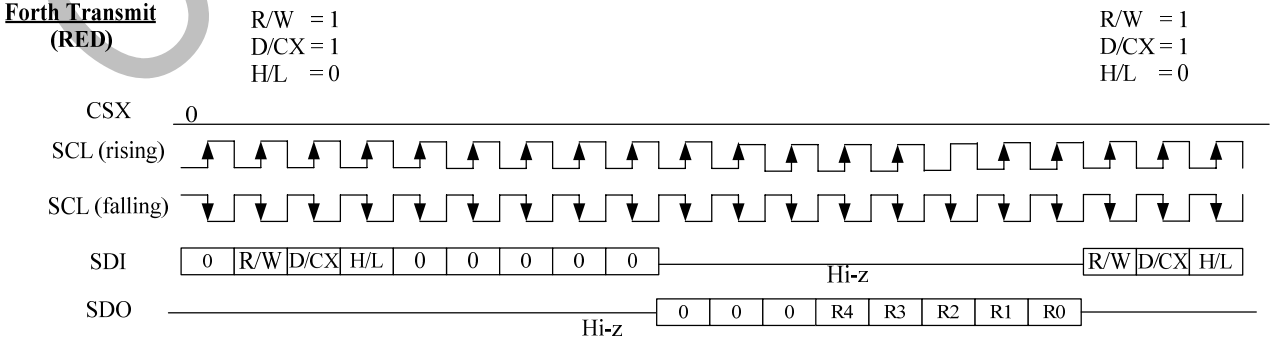

**Second Transmit**




**Third Transmit (Dummy)**




**Forth Transmit (RED)**

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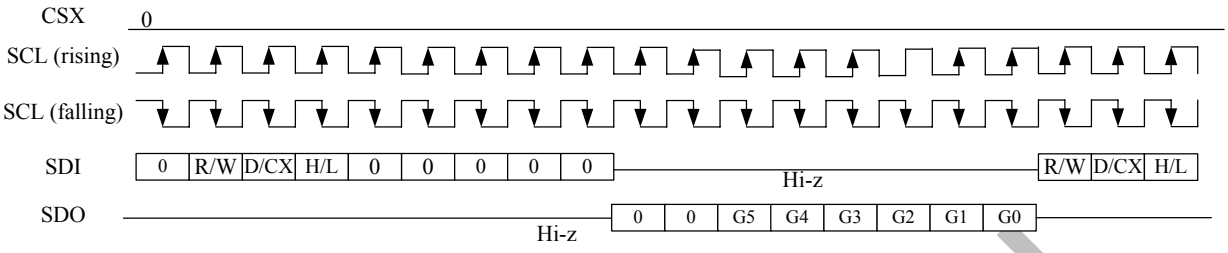
**Fifth Transmit (GREEN)**

R/W = 1
D/CX = 1
H/L = 0

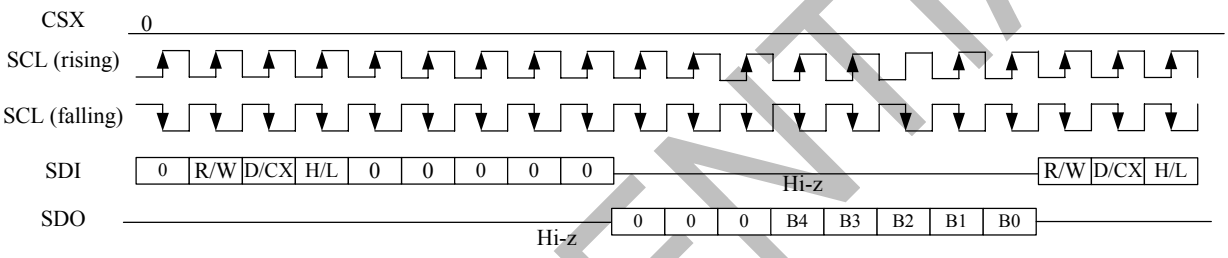
R/W = 1
D/CX = 1
H/L = 0




**Sixth Transmit (BLUE)**

R/W = 1
D/CX = 1
H/L = 0

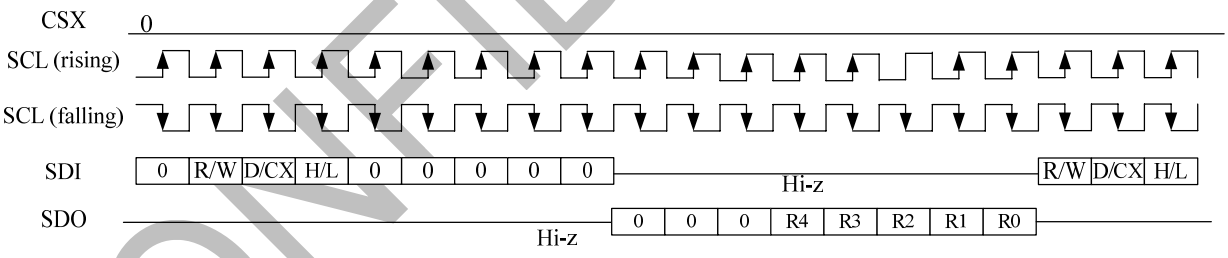
R/W = 1
D/CX = 1
H/L = 0




**Seventh Transmit (RED)**

R/W = 1
D/CX = 1
H/L = 0

R/W = 1
D/CX = 1
H/L = 0

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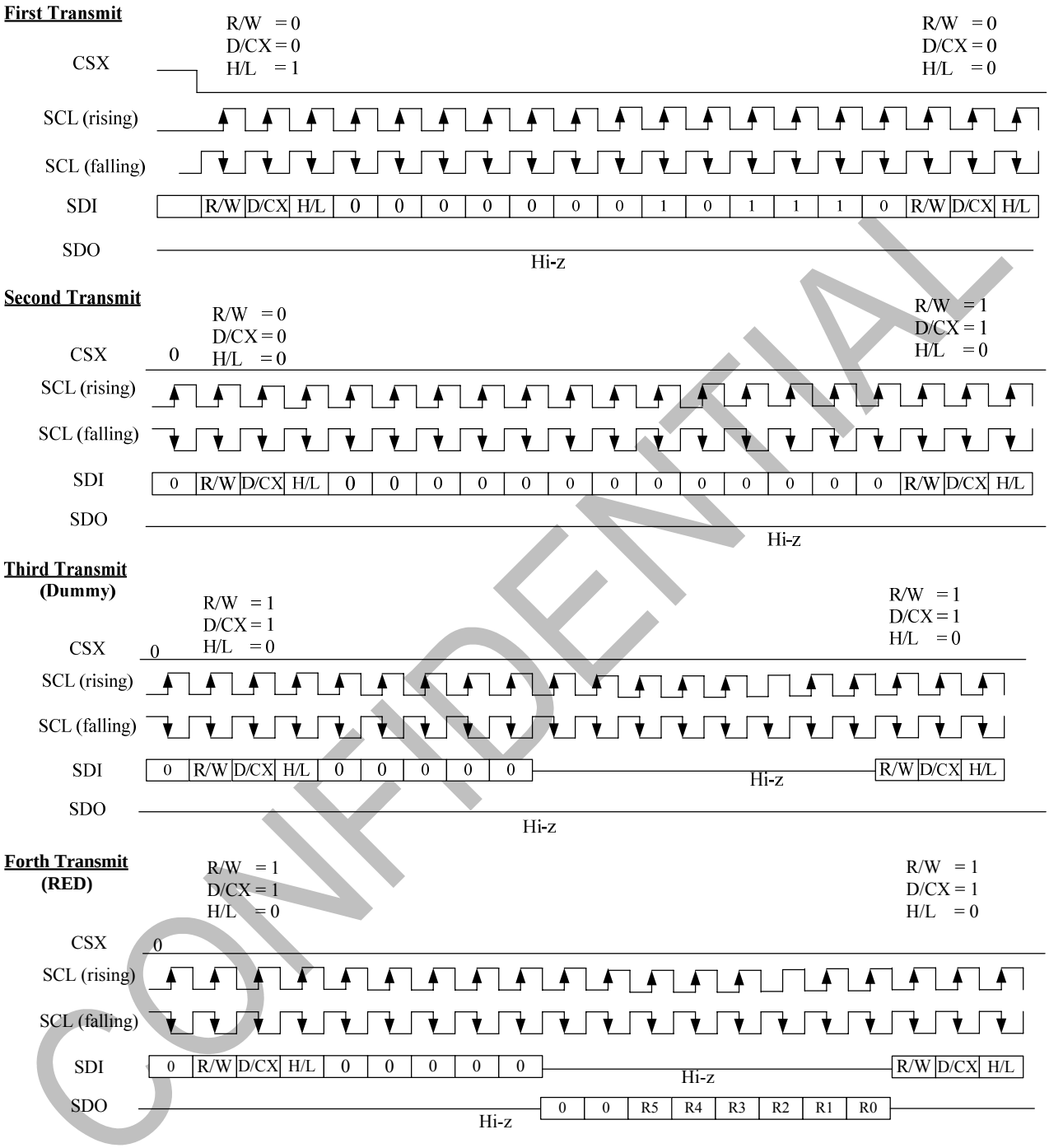
SRAM read: 262K colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)

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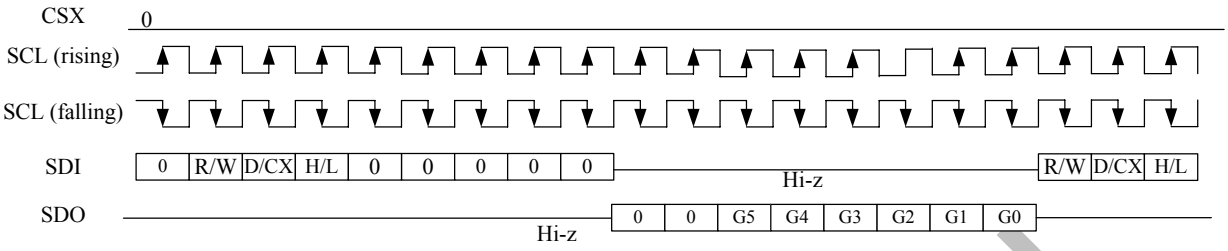
**Fifth Transmit (GREEN)**

R/W = 1
D/CX = 1
H/L = 0

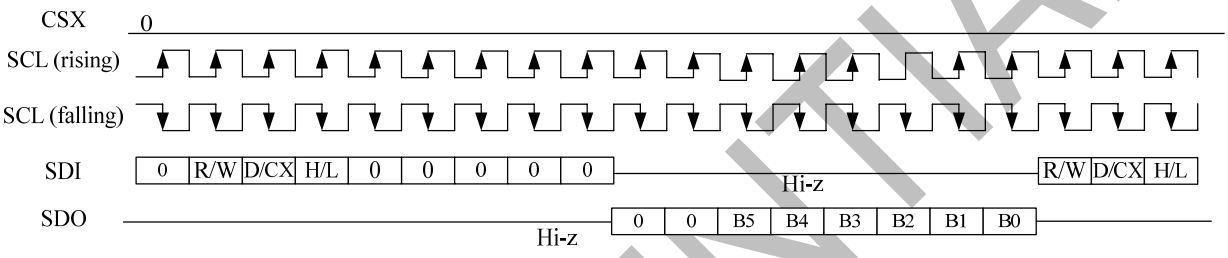
R/W = 1
D/CX = 1
H/L = 0




**Sixth Transmit (BLUE)**

R/W = 1
D/CX = 1
H/L = 0

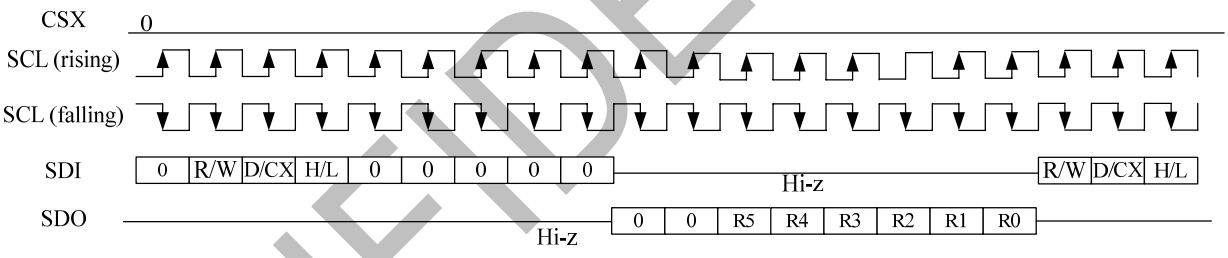
R/W = 1
D/CX = 1
H/L = 0




**Seventh Transmit (RED)**

R/W = 1
D/CX = 1
H/L = 0

R/W = 1
D/CX = 1
H/L = 0

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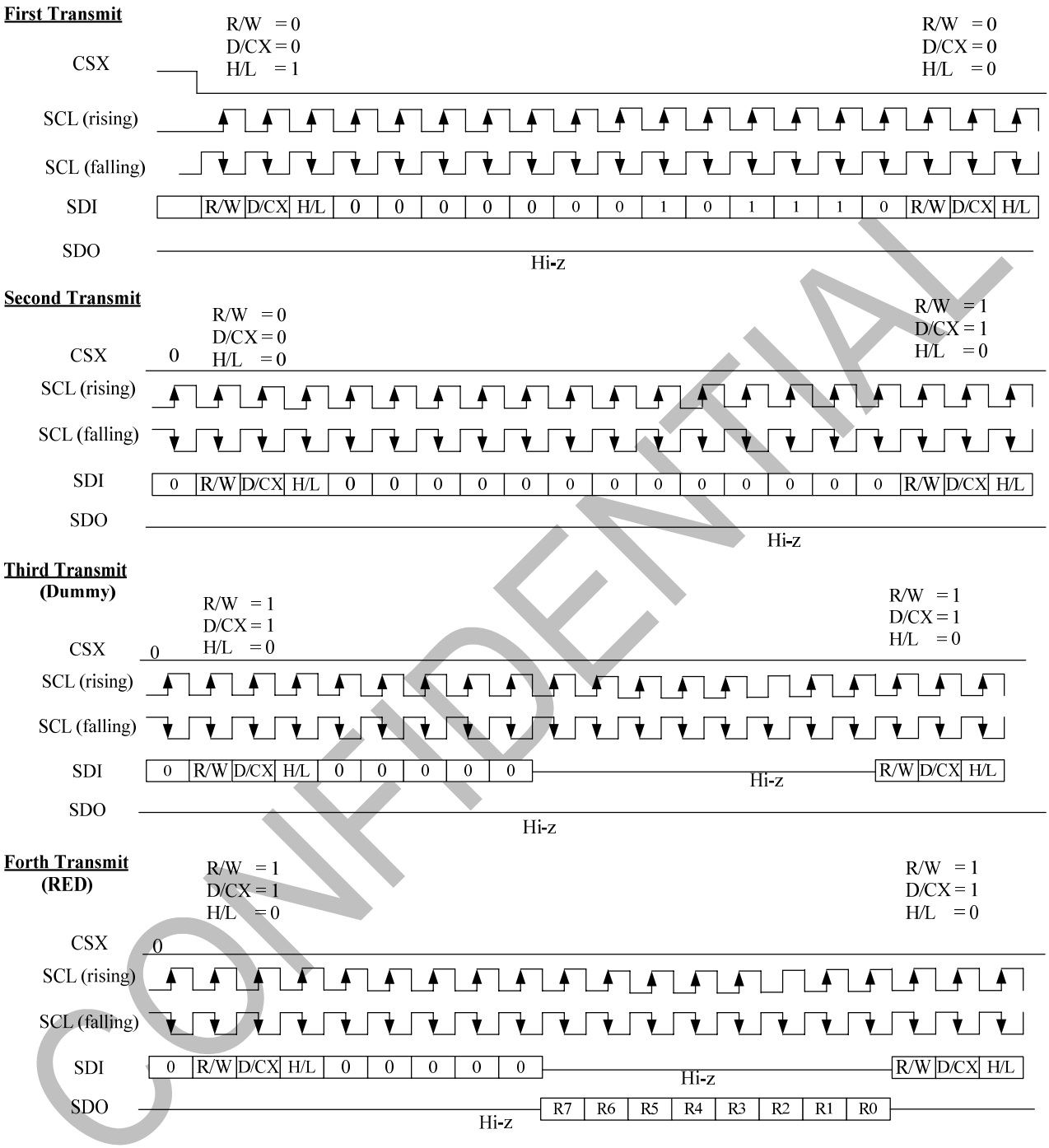
SRAM read: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)

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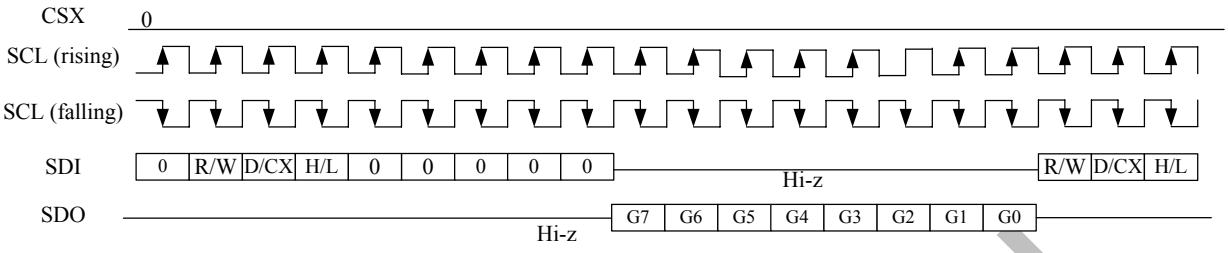
**Fifth Transmit (GREEN)**

R/W = 1
D/CX = 1
H/L = 0

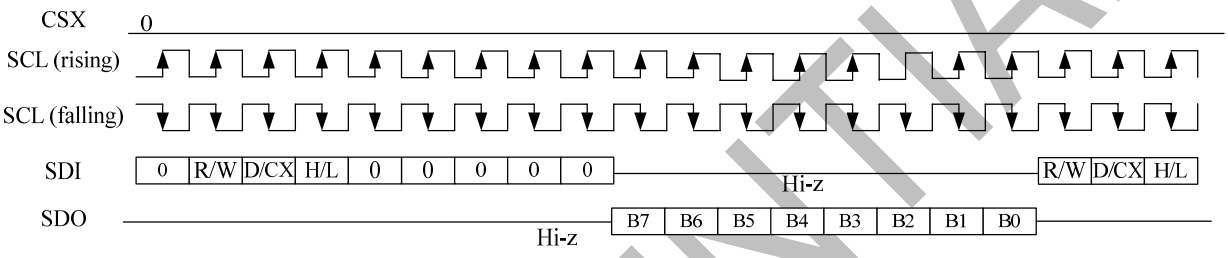
R/W = 1
D/CX = 1
H/L = 0




**Sixth Transmit (BLUE)**

R/W = 1
D/CX = 1
H/L = 0

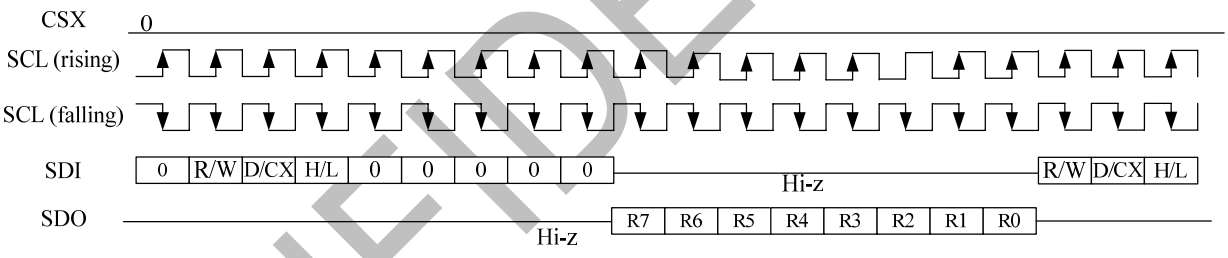
R/W = 1
D/CX = 1
H/L = 0




**Seventh Transmit (RED)**

R/W = 1
D/CX = 1
H/L = 0

R/W = 1
D/CX = 1
H/L = 0

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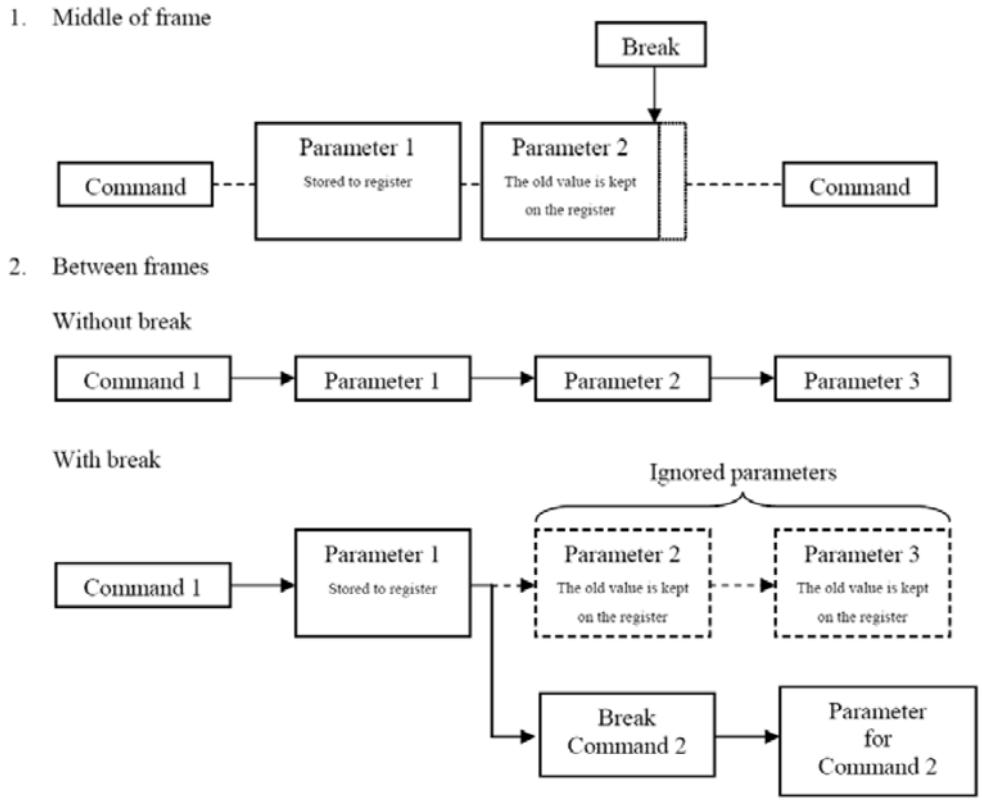
### 7.3.3 Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.




Break can be e.g. another command or noise pulse.

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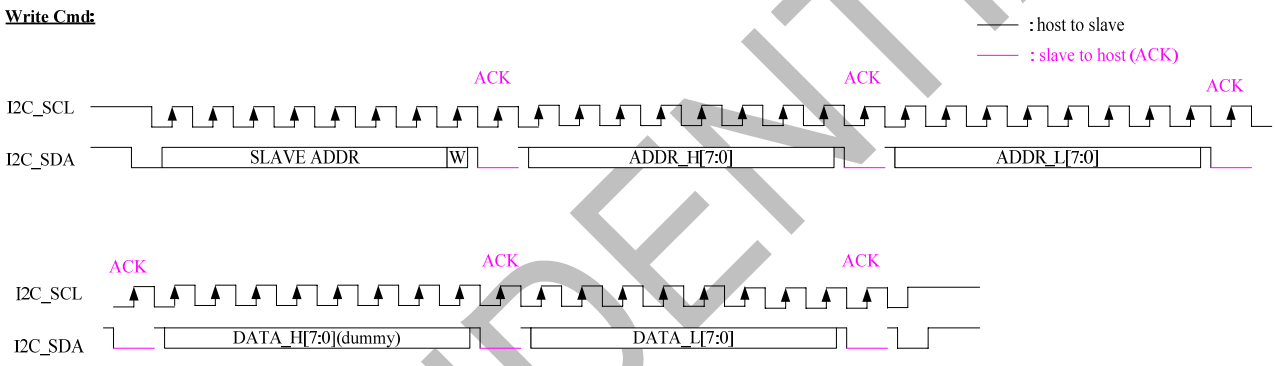
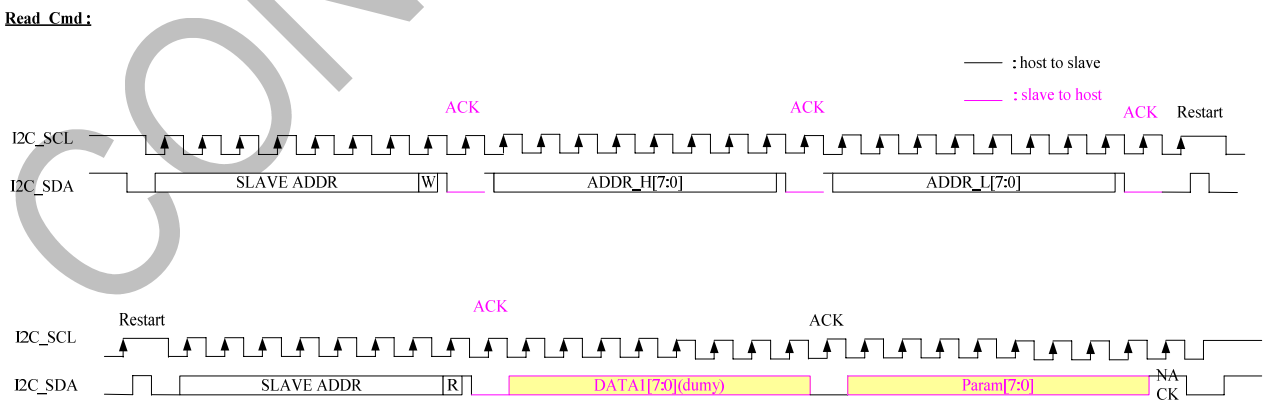
### 7.4 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

The I2C interface write command sequences are described in the following figure.




The I2C interface read command sequences are described in the following figure.

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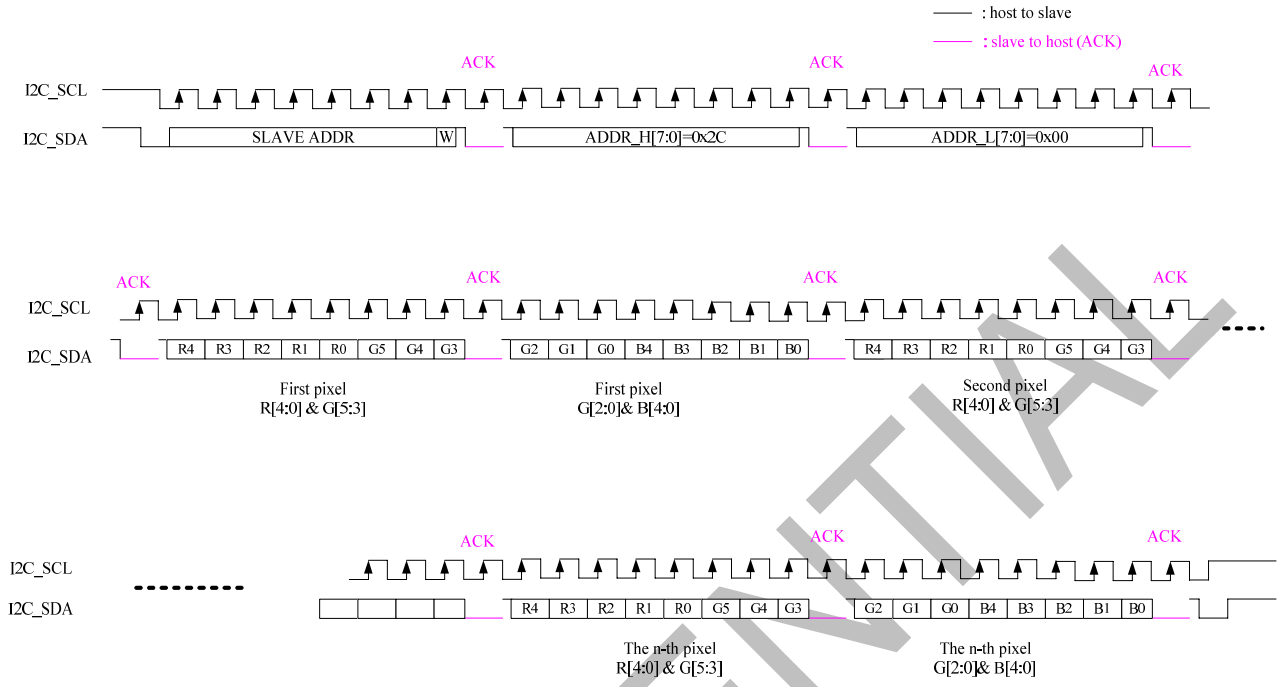
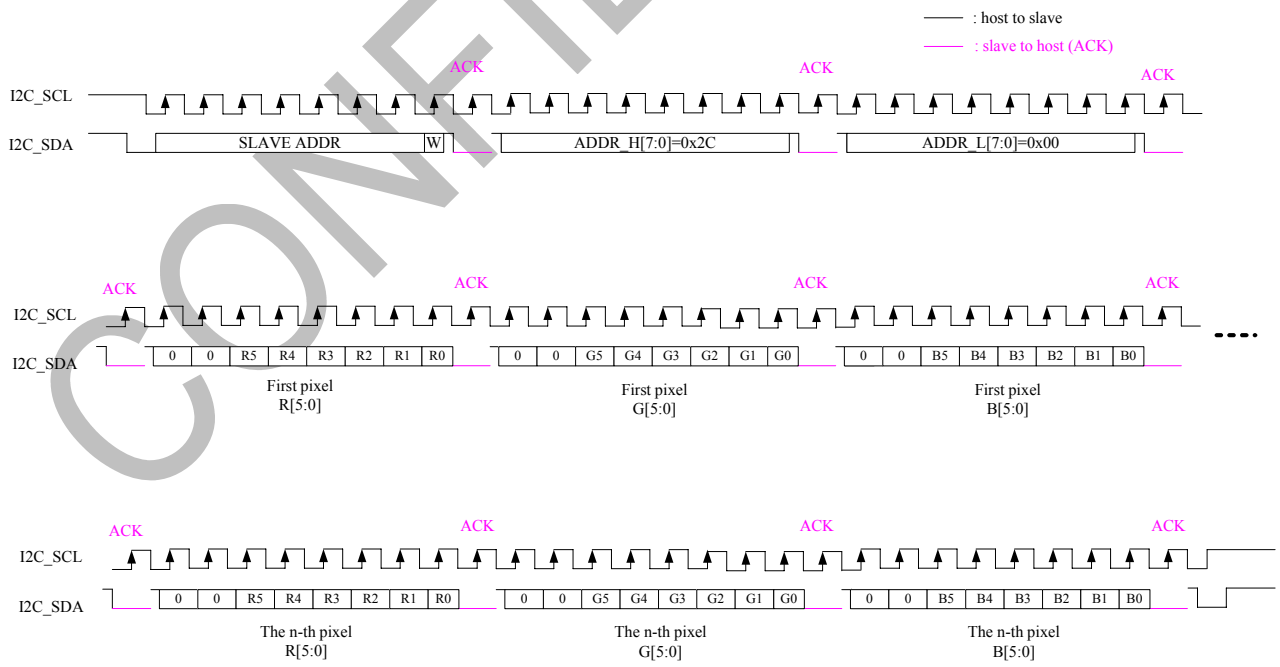
The I2C interface write data sequences are described in the following figure.

SRAM write: 65k colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)




SRAM write: 262k colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)

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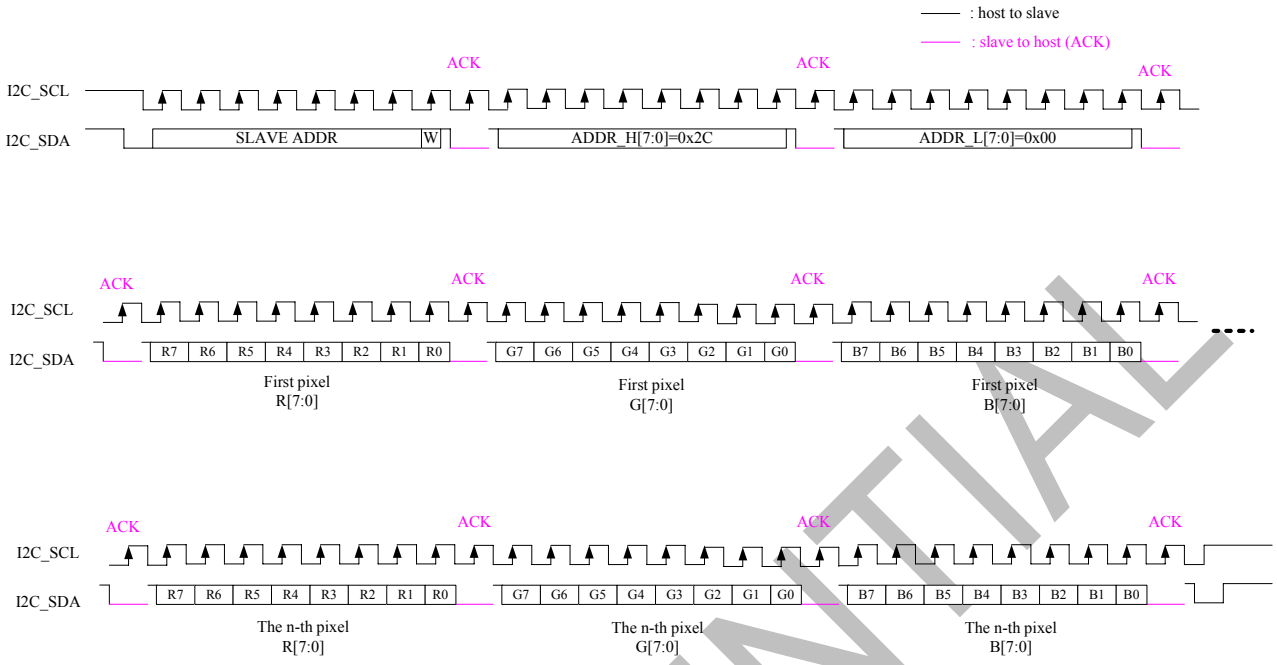
SRAM write: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)

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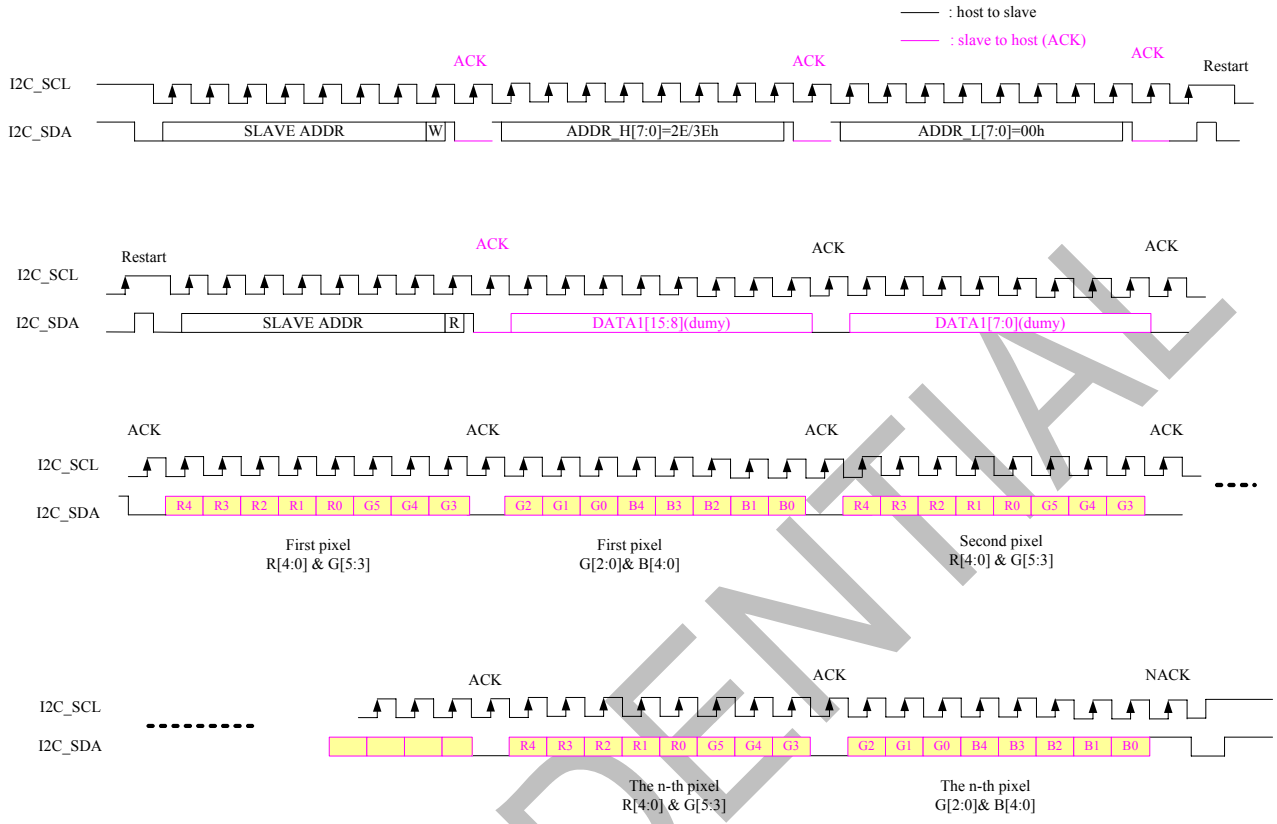
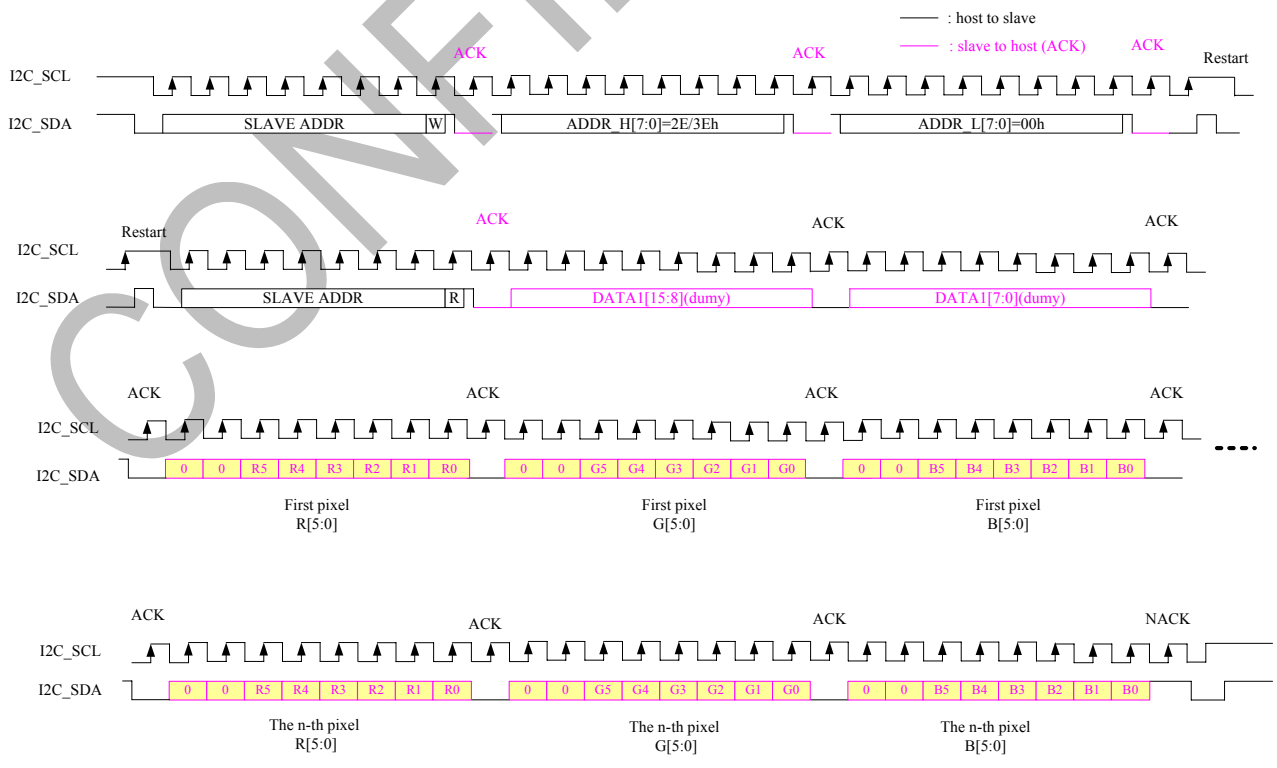
The I2C interface read data sequences are described in the following figure.

SRAM read: 65k colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)




SRAM read: 262k colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)

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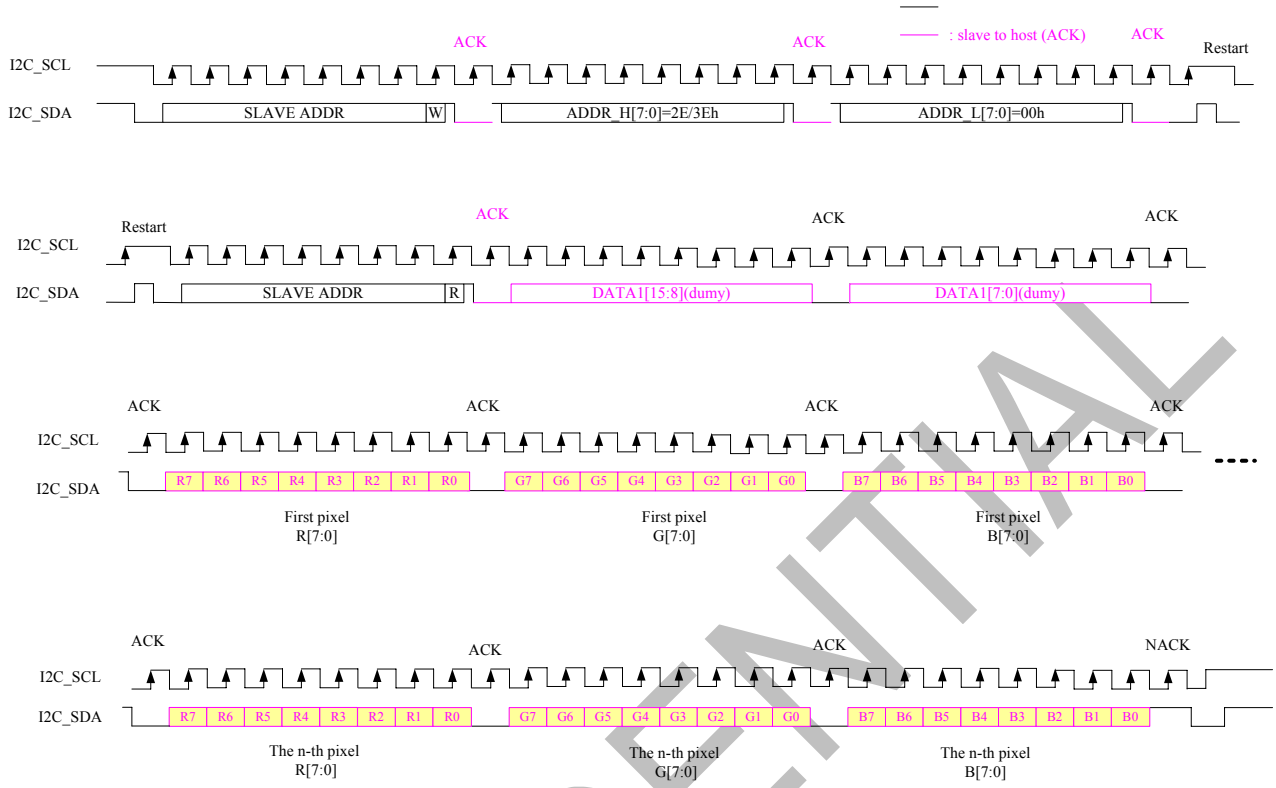
SRAM read: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)

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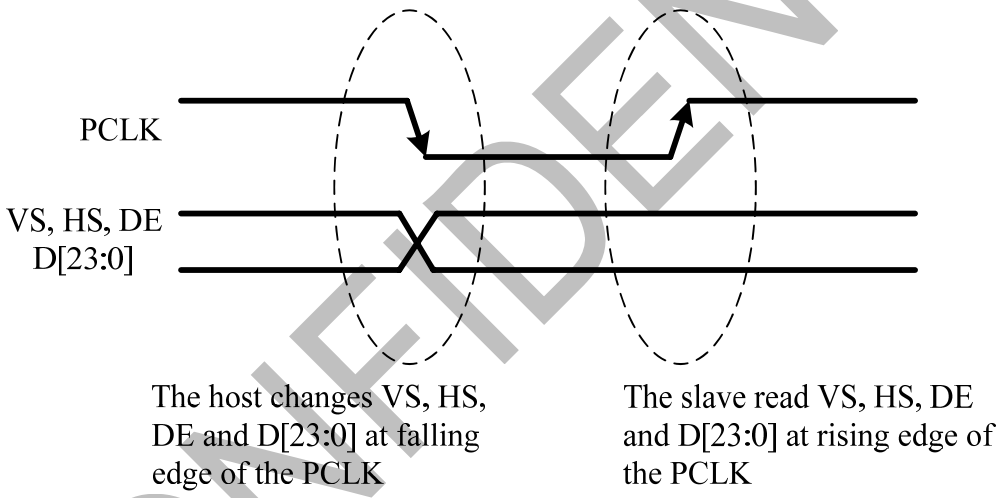
### 7.5 Display Pixel Interface (DPI)

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image. Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16, 18 or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

DPI signals are described in the follow figure.




DPI Interface data bus format: (Selected by VIPF[3:0])

| VIPF | DB 23 | DB 22 | DB 21 | DB 20 | DB 19 | DB 18 | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 | color |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | | | | R[4] | R[3] | R[2] | R[1] | R[0] | | | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | | | | B[4] | B[3] | B[2] | B[1] | B[0] | 65K |
| 6 | | | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | | | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | | | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | 262K |
| 7 | R[7] | R[6] | R[5] | R[4] | R[3] | R[2] | R[1] | R[0] | G[7] | G[6] | G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | 16.7M |

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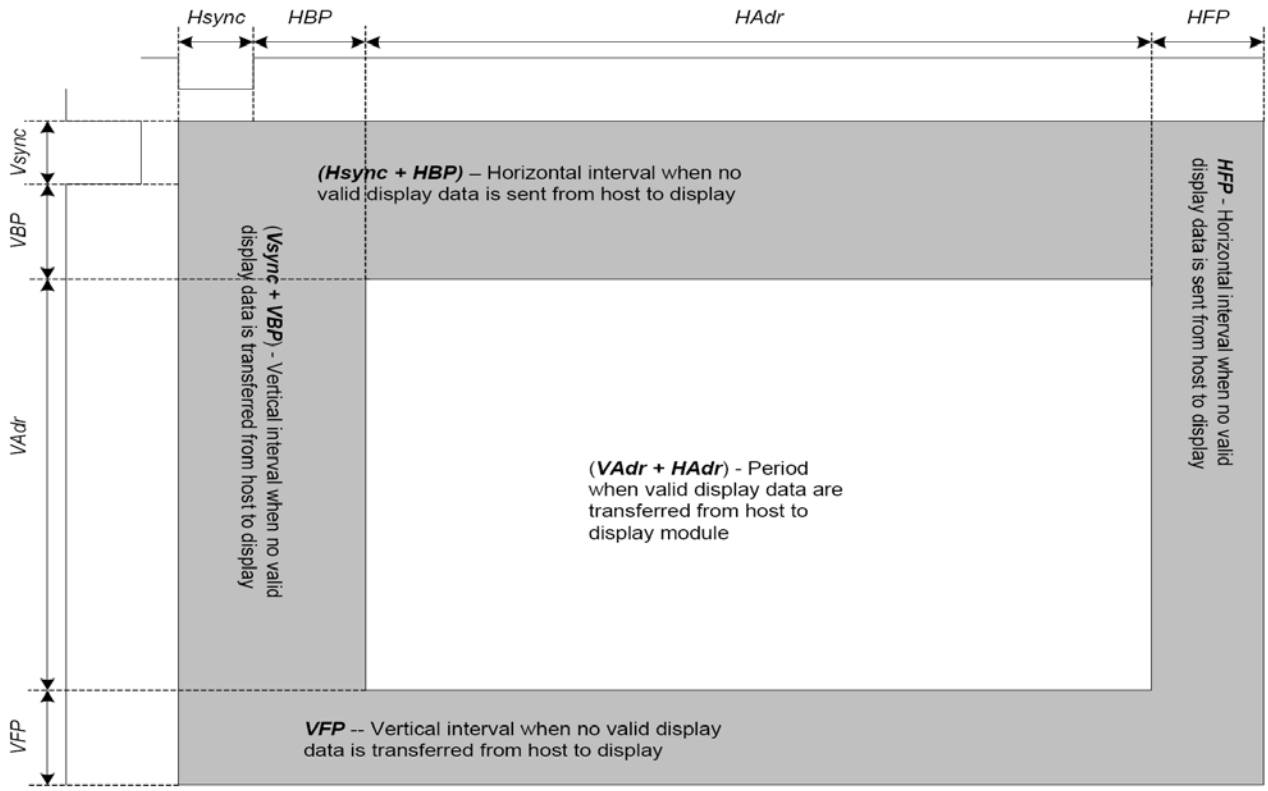
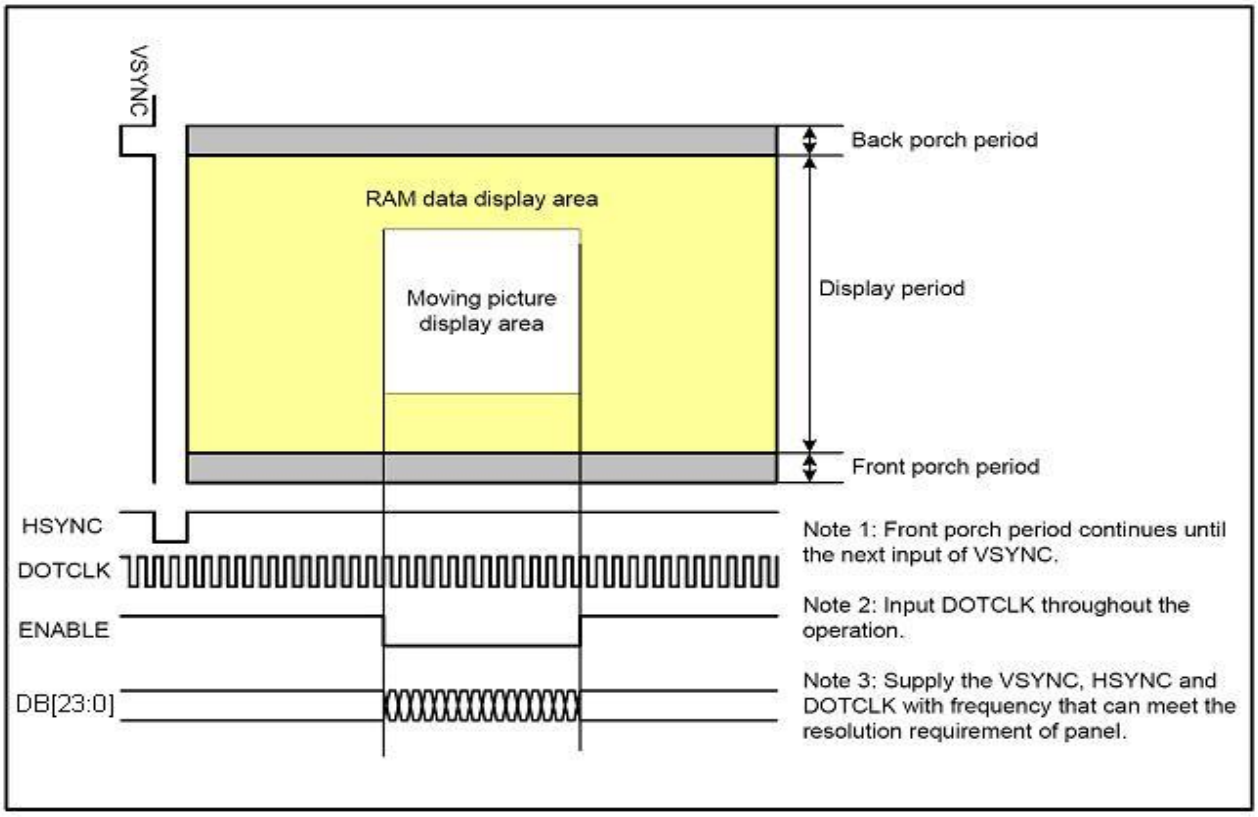
DPI Interface Timing Chart.

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### 7.6 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

RM68120 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. RM68120 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM68120 Configuration:

| Lane Pair | MCU(Master)　RM68120(Slave) |
|---|---|
| Clock Lane | Unidirectional Lane<br>Clock only |
| Data Lane 0 | Bi-directional Lane<br>➢ Forward High-speed<br>➢ Bi-directional Escape Mode<br>➢ Bi-directional LPDT |
| Data Lane 1 | Unidirectional Lane<br>➢ Forward High-Speed<br>➢ Escape Mode |

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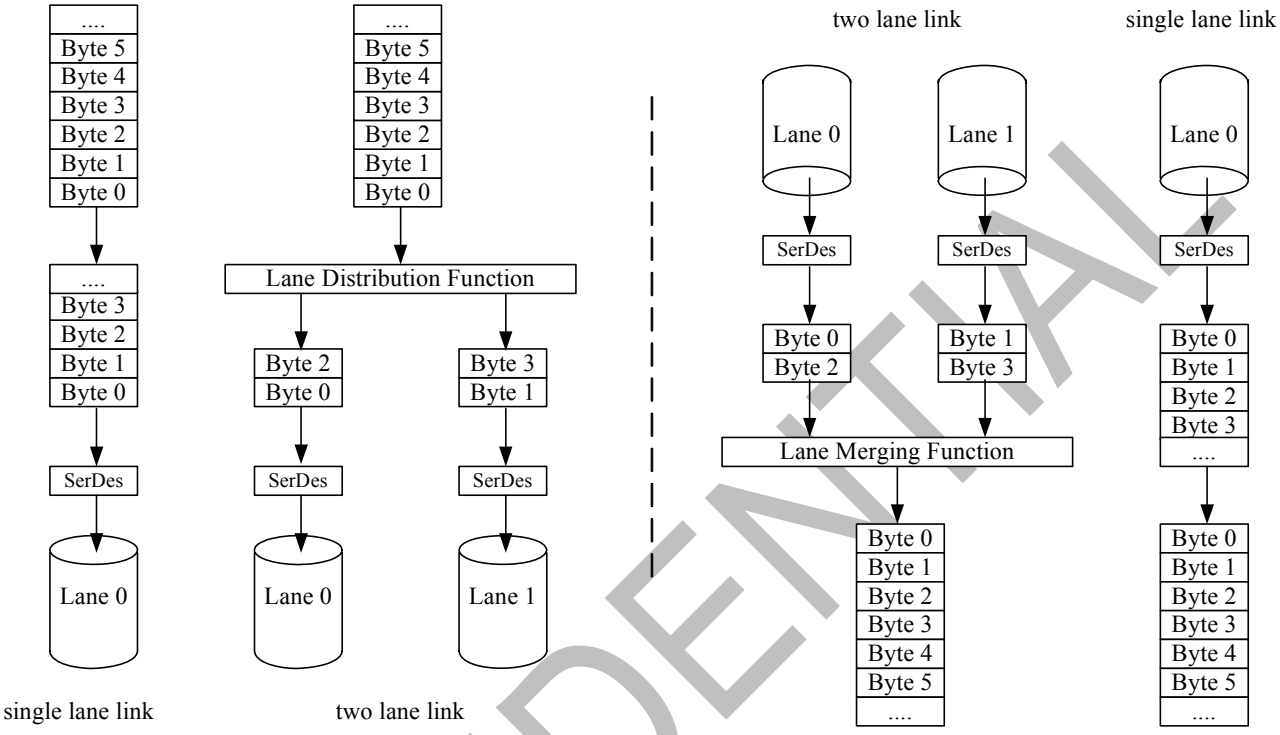
### 7.6.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.




There are two kinds of packets, **short packet and long packet**.

- Short packet structure:

  LP-11: low power mode

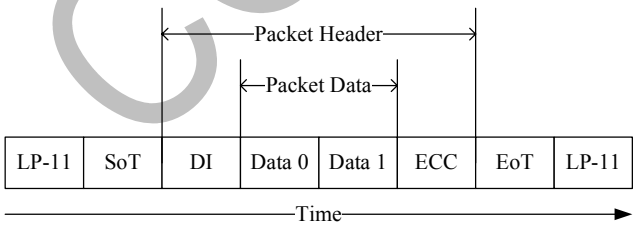
  SoT: start of transmission

  DI: data identification

  Data 0, Data1: packet data

  ECC: error correction code

  EoT: End of Transmission

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DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

| Virtual Channel (VC) | | Data Type (DT) | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

- Long packet structure:

LP-11: low power mode

SoT: start of transmission

DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission

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### 7.6.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

| Data Type | Data Type binary | Description | Packet Size |
|---|---|---|---|
| 01h | 00 0001 | Sync Event, V Sync Start | Short |
| 11h | 01 0001 | Sync Event, V Sync End | Short |
| 21h | 10 0001 | Sync Event, H Sync Start | Short |
| 31h | 11 0001 | Sync Event, H Sync End | Short |
| 08h | 00 1000 | End of Transmission packet (EoTp) | Short |
| 02h | 00 0010 | Color Mode (CM) Off Command | Short |
| 12h | 01 0010 | Color Mode (CM) On Command | Short |
| 22h | 10 0010 | reserved | Short |
| 32h | 11 0010 | reserved | Short |
| 03h | 00 0011 | reserved | Short |
| 13h | 01 0011 | Generic Short WRITE, 1 parameter | Short |
| 23h | 10 0011 | Generic Short WRITE, 2 parameters | Short |
| 04h | 00 0100 | reserved | Short |
| 14h | 01 0100 | Generic READ, 1 parameter | Short |
| 24h | 10 0100 | Generic READ, 2 parameters | Short |
| 05h | 00 0101 | DCS Short WRITE, no parameters | Short |
| 15h | 01 0101 | DCS Short WRITE, 1 parameter | Short |
| 06h | 00 0110 | DCS READ, no parameters | Short |
| 37h | 11 0111 | Set Maximum Return Packet Size | Short |
| 09h | 00 1001 | Null Packet, no data | Long |
| 19h | 01 1001 | Blanking Packet, no data | Long |
| 29h | 10 1001 | Generic Long Write | Long |
| 39h | 11 1001 | DCS Long Write/write_LUT Command Packet | Long |
| 0Eh | 00 1110 | Packed Pixel Stream, 16-bit RGB, 5-6-5 Format | Long |
| 1Eh | 01 1110 | Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 2Eh | 10 1110 | Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format | Long |
| 3Eh | 11 1110 | Packed Pixel Stream, 24-bit RGB, 8-8-8 Format | Long |

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- Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

- EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM68120 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

- Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

- Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

- DCS commands
  - DCS short write command

    DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

  - DCS read commands

    The commands are used to request data from s display module.

  - DCS Long Write / write_LUT command

    The commands are used to send larger blocks of data to a display module.

  - Maximum return packet size

    This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

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- Null Packet

  This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

- Blanking Packet

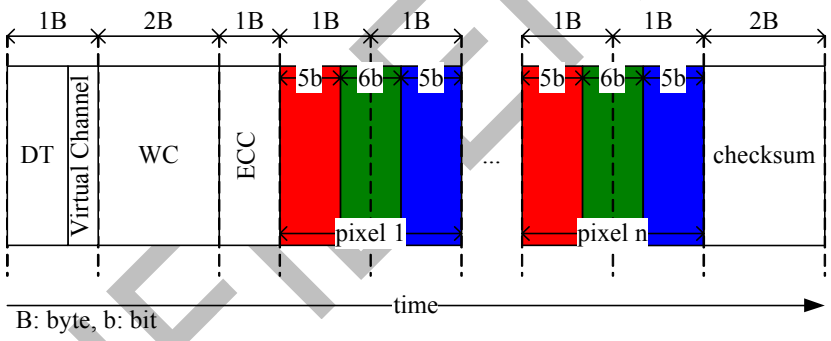
  A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

- Generic Long Write

  This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

- Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

  The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

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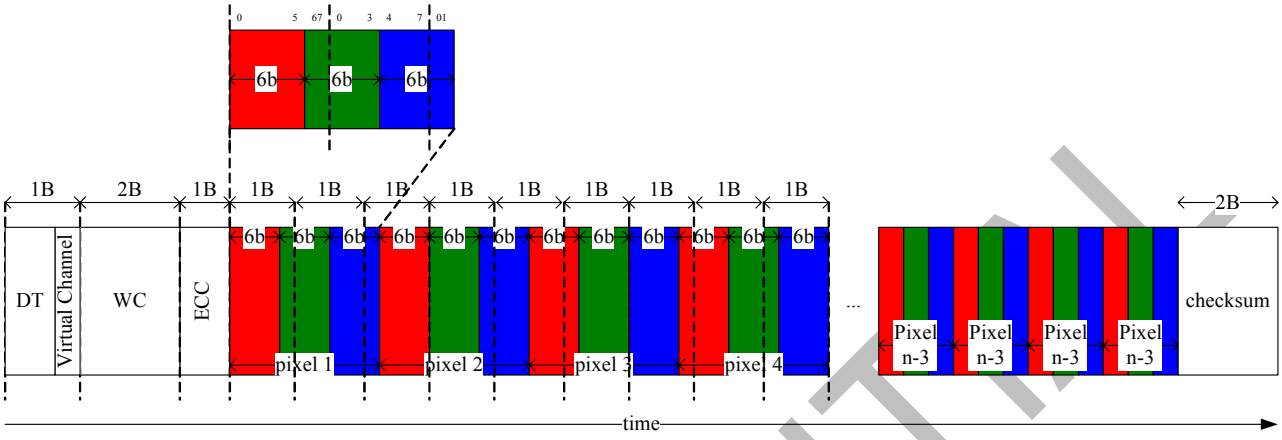
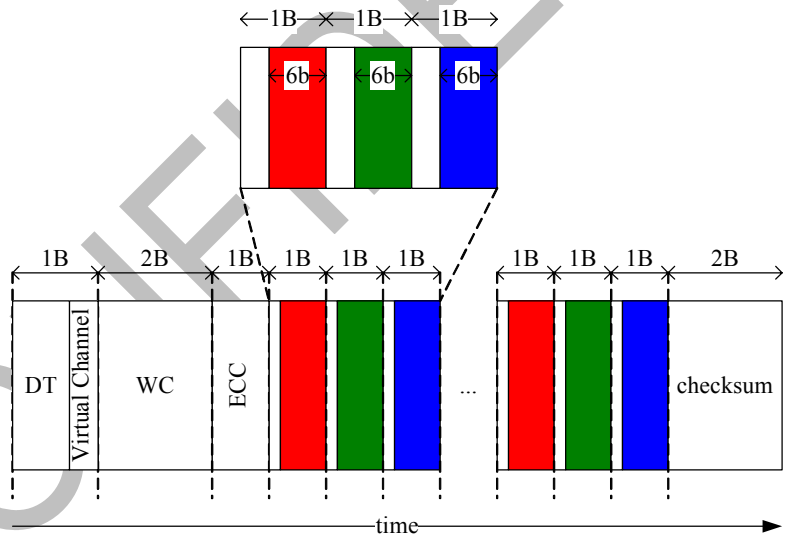
- Packet pixel stream, 18-bit format, Data Type: 01 1110

  The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.




- Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

  This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.

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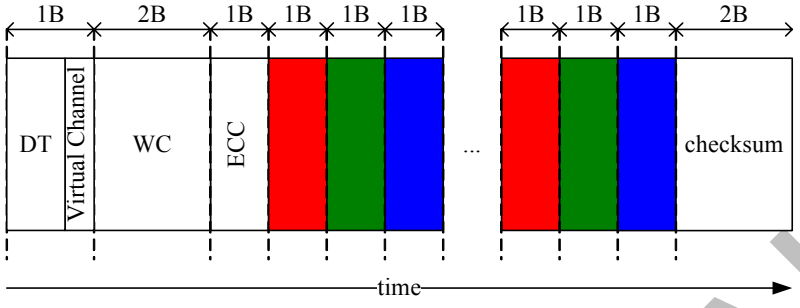
- Packet pixel stream, 24-bit format, Data Type: 11 1110

  The pixel format is eight bits red, eight bits green and eight bits blue.

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### 7.6.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission. Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

- Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.
- Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.
- Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.
- Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.
- Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.
- Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.
- Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.
- Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.
- Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.
- Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error

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is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

**Error Report Format**

The following table shows the bit assignment for all error report.

| Bit | Description |
|---|---|
| 0 | SoT Error |
| 1 | SoT Sync Error |
| 2 | EoT Sync Error |
| 3 | Escape Mode Entry Command Error |
| 4 | Low-Power Transmit Sync Error |
| 5 | HS Receive Timeout Error |
| 6 | False Control Error |
| 7 | Reserved |
| 8 | ECC Error, single-bit (detected and corrected) |
| 9 | ECC Error, multi-bit (detected, not corrected) |
| 10 | Checksum Error (Long packet only) |
| 11 | DSI Data Type Not Recognized |
| 12 | DSI VC ID Invalid |
| 13 | reserved |
| 14 | reserved |
| 15 | reserved |

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**Peripheral-to-Processor Transaction – Detail Format Description**

The following list is the complete set of peripheral-to-processor data types.

| Data type, hex | Data type binary | Description | Packet size |
|---|---|---|---|
| 02h | 00 0010 | Acknowledge and error report | short |
| 08h | 00 1000 | reserved | short |
| 11h | 01 0001 | GEN short read reponse, 1byte returned | short |
| 12h | 01 0010 | GEN short read reponse, 2bytes returned | short |
| 1Ah | 01 1010 | Generic long read reponse | long |
| 1Ch | 01 1100 | DCS long read reponse | long |
| 21h | 10 0001 | DCS short read reponse, 1byte returned | short |
| 22h | 10 0010 | DCS short read reponse, 2bytes returned | short |

- Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.
- Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

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### 7.6.4 Notice

1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.

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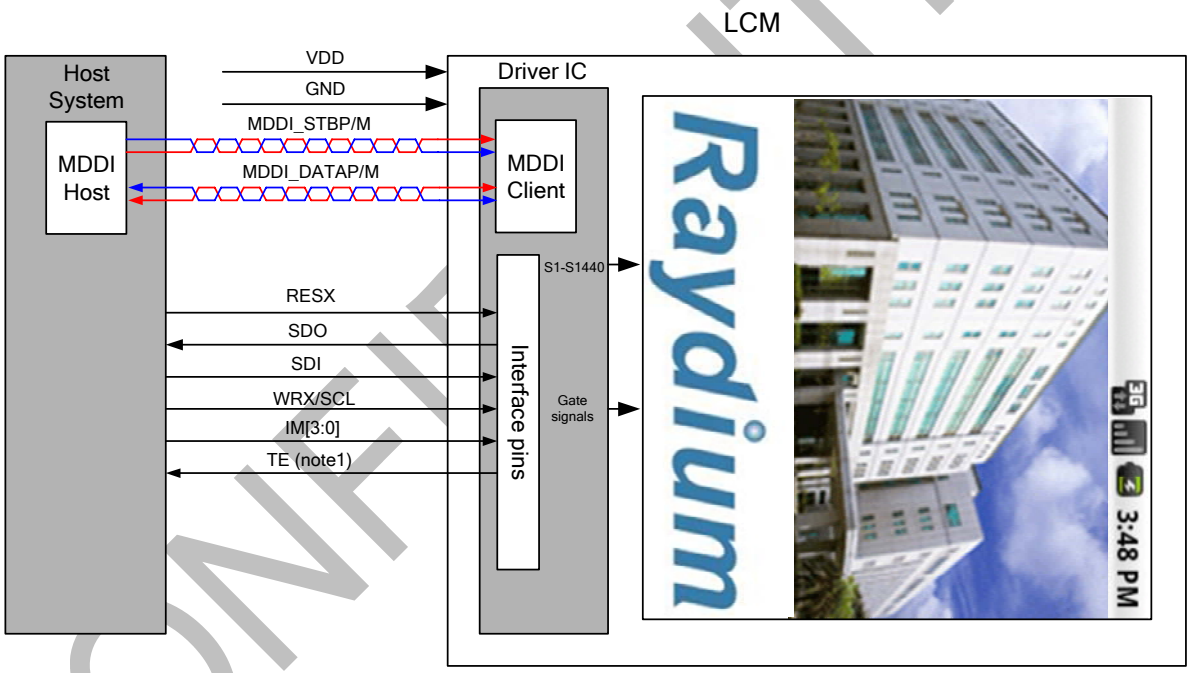
### 7.7 MDDI Interface

The RM68120 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following lines: DATA0_P/M, DATA1_P/M and STB_P/M. The specifications of MDDI supported by the RM68120 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA).

The RM68120 offers the bi-direction link to use for the register and display data read / write.

For power saving, the RM68120 offers both hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption.

The RM68120 supports the MDDI Type-I and Type-II of the MDDI specifications Version 1.2 and the application diagram is illustrated as follow.




Notes:

1. Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effect.
2. When enter to the MDDI interface from other interface, the Host needs to wait 100ms and can start to send any packet. For example wake up packet.
3. After shutting down the MDDI interface the Host needs to wait 500ns and can start to send wake up packet to wake up the MDDI link.
4. The terminal resistors are embedded between MDDI_DATA0_P/M, MDDI_DATA1_P/M and MDDI_STB_P/M.

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### 7.7.1 MDDI Link Protocol

The RM68120's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol.

DO NOT send any packets that are not supported by the RM68120 into a system containing the RM68120.

Supported MDDI packets are as follows:

| RM68120 MDDI packets | Packet Name | Packet Type | Direction | Supported Type |
|---|---|---|---|---|
| Link Control Packet | Sub-frame header packet | 15359 (0x3BFF) | Forward | Type I/Type II |
| | Filler packet | 0 | Forward/Reverse | Type I/ Type II (Forward) Type I Only (Reverse) |
| | Link Shutdown packet | 69 (0x45) | Forward | Type I/Type II |
| | Reverse link encapsulation packet | 65 (0x41) | Forward | Type I Only |
| | Round-trip delay measurement packet | 82 (0x52) | Forward | Type I/Type II |
| | Forward link skew calibration packet | 82 (0x52) | Forward | Type I/Type II |
| Client Status and Control Packet | Client capability packet | 66 (0x42) | Reverse | Type I Only |
| | Client request and status packet | 70 (0x46) | Reverse | Type I Only |
| | Register access packet | 146 (0x92) | Forward/Reverse | Type I/ Type II (Forward) Type I Only (Reverse) |
| Basic Media Stream Packet | Video stream packet | 16 (0x10) | Forward | Type I/Type II |
| | Flexible video stream packet | 20 (0x14) | Forward | Type I/Type II |
| | Windowless video stream packet | 22 (0x16) | Forward | Type I/Type II |

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### 7.7.2 MDDI Link Packet Descriptions

**Sub-frame Header Packet**

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub-frame Header Packet

| Packet Length | Packet Type =0x3bff | Unique word =0x005a | Reversed 1 | Sub-frame Length | Protocol Version | Sub-frame Count | Media-frame Count | CRC |
|---|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0x3bff

Unique Word: unique word is 0x005a

Reserved 1: not used (set to zero)

Sub-frame Length: specify the number of bytes per sub-frame

Protocol version: set to zero

- Bit [15:2] – Reserved for future expansion. These should be set to all zero.
- Bits[1:0] – Sub-frame operational mode

"00" – Sub-frame lengths strictly followed.

"01" – Sub-frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame length has been transmitted.

"10" – Sub-frame lengths are unlimited. No more sub-frame packets are required tobe transmitted after the first sub-Frame packet at startup.

Sub-frame Count: specify the number of sub-frame header packet

Media-frame Count: specify the number of media-frames

CRC: error check

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**Filler Packet**

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

Filler Packet

| Packet Length | Packet Type=0 | Filler Bytes (all zero recommended) | CRC |
|---|---|---|---|
| 2 bytes | 2 bytes | (Packet Length – 4) bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0

Filler Bytes: set to zero

CRC: error check

**Link Shutdown Packet**

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.

Link Shutdown Packet

| Packet Length | Packet Type=69 | CRC | All Zero |
|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | (Packet Length – 4) bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 69

CRC: error check

All Zero: set to zero (Type I: size is 16 bytes, Type II: size is 32 bytes)

**Reverse Link Encapsulation Packet**

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.

Reverse Link Encapsulation Packet

| Packet Length | Packet Type=65 | hClient ID | Reversed Link Flags | Reverse Rate Divisor | Turn-Around 1 Length | Turn-Around 2 Length |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 1 byte | 1 byte | 1 byte | 1 byte |

| Parameter CRC | All Zero 1 | Turn-Around 1 | Reversed Data Packets | Turn-Around 2 | All Zero 2 |
|---|---|---|---|---|---|
| 2 bytes | 8 bytes | x bytes | (Packet Length –x –y -26) bytes | y bytes | 8 bytes |

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Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 65

hClient ID: set to zero

Reverse Link Flags:

- Bit 0 – 0: No packet request
  1: Host needs the Client Capability Packet
- Bit 1 – 0: No packet request
  1: Host needs the Client Request and Status Packet
- Bit [7:2] – set to zero

Reverse Rate Divisor: reverse data rate = reverse link data clock

Turn-Around 1 Length: the length of Turn-Around 1 is the forward link data rate

Turn-Around 2 Length: the length of Turn-Around 2 is determined by Round-trip delay of the link

Parameter CRC: error check

All zero: set to zero

Turn-Around 1: First turn-around period

Reverse Data Packets: A series of data packets transferred from the client to host

Turn-Around 2: The second turn-around period

**Round-Trip Delay Measurement Packet**

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

Round Trip Measurement Packet

| Packet Length | Packet Type=82 | hClient ID | Parameter CRC |
|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 byte |

| Guard Time 1 | Measurement Period | All Zero | Guard Time 2 |
|---|---|---|---|
| 64 bytes | 64 bytes | 2 bytes | 64 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 82

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hCilent ID: set to zero

Parameter CRC: error check

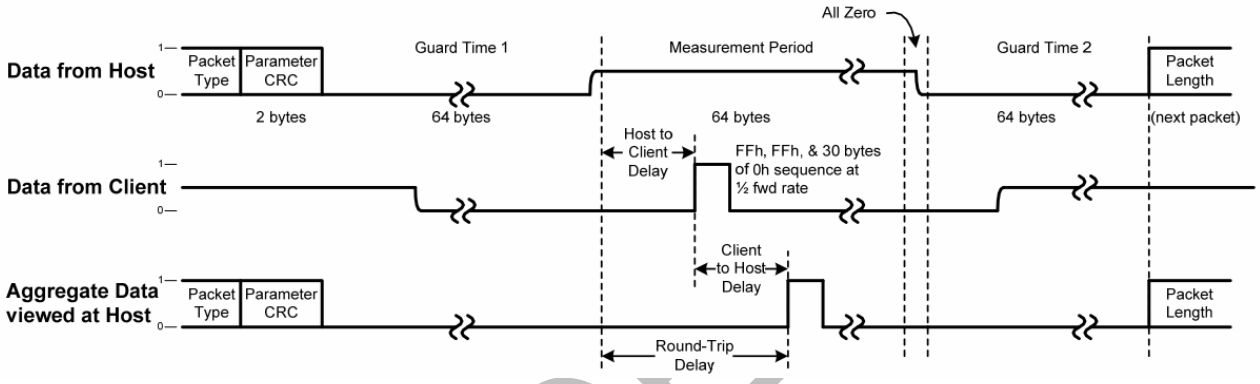
Guard Time 1: allow overlap of the host and client

Measurement Period: a 64 bytes window to allow the client to respond

All Zero: set to zero

Guard Time 2: allow overlap of the measurement period by the client

The timing of events during the Round-Trip Delay Measurement Packet illustrates as follow.




**Forward Link Skew Calibration Packet**

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_DATA signals with respect to the MDDI_STB signal. Without delay skew compensation the maximum data rate must be limited to account for the worst-case variation in these delays. It is recommended that this packet only be sent when the forward link data rate is configured to 50 Mbps or lower. After sending this packet to calibrate the client the data rate may be stepped up above 50 Mbps. With the data rate set too high during the skew calibration process the client might synchronize to an alias of the bit period which would cause the delay skew compensation setting to be off by more than one bit time, resulting in erroneous data clocking. The greatest possible Interface Type must be selected prior to sending the Forward Link Skew Calibration Packet so that all existing data bits are calibrated. The client must indicate its ability to support the Forward Link Skew Calibration Packet via bit 19 of Client Feature Capability Indicators field of the Client Capability Packet.

Prior to performing skew calibration the host must not send data faster than the rate specified by the Pre-calibration Data Rate Capability field of the Client Capability Packet. However, after calibration is performed, the host may send data up to the rate defined by the Post-calibration Data Rate Capability field. It is recommended that the host send the Forward Link Skew Calibration Packet at regular intervals to correct

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changes in the relative delay between the different signal pairs due to changes in temperature.

**Forward Link Skew Calibration Packet**

| Packet Length | Packet Type=83 | hClient ID | Parameter CRC | All Zero 1 | Calibration Data Sequence | All Zero 2 |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | Pacet Length – 22 bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 83

hCilent ID: set to zero

Parameter CRC: error check from packet length to the hClient ID.

All Zero 1:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field ensures that there will be a transition on MDDI_STB at the beginning of the Calibration Data Sequence field. It also provides sufficient time for the client core logic to change the mode of the clock recovery circuit from using the XOR of MDDI_Data0 and MDDI_STB to simply using MDDI_STB as the recovered clock.

Calibration Data Sequence:

a data sequence that causes the MDDI_Data signals to toggle at every data period. The length of the Calibration Data Sequence field is determined by the interface type being used on the forward link. During the Calibration Data Sequence the MDDI host controller sets all MDDI_Data signals equal to the strobe signal. The client clock recovery circuit must use only MDDI_STB rather than MDDI_STB XOR MDDI_Data0 to recover the data clock while the Calibration Data Sequence field is being received by the client. Depending on the exact phase of MDDI_STB at the beginning of the Calibration Data Sequence field the Calibration Data Sequence will be one of the following based on the interface Type being used when this packet is sent:

- Type 1 – (64 byte data sequence) AAh, AAh … or 55h, 55h…
- Type 2 – (128 byte data sequence) CCh, CCh … or 33h, 33h…

All Zero 2:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field provides sufficient time for the client core logic to change the mode of the clock recovery circuit back to the original state, from using MDDI_STB as the recovered clock to using the XOR of MDDI_Data0 and MDDI_STB.

**Client Capability Packet**

It is recommended that the client send a Client Capability Packet to the host after forward link

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synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

Client Capability Packet

| Packet Length | Packet Type=66 | cClient ID | Protocol Version | Min Protocol Version | Pre-calibration Data Rate Capability | Interface Type Capability |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 1 byte |

| Number of Alt Display | Post-calibration Data Rate Capability | Bitmap Width | Bitmap Height | Display Window Width | Display Window Height | Color Map Size |
|---|---|---|---|---|---|---|
| 1 byte | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 4 bytes |

| Color Map RGB Width | RGB Capability | Monochrome Capability | Reversed 1 | Y Cb Cr Capability | Bayer Capability | Revered 2 |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 1 byte | 1 byte | 2 bytes | 2 bytes | 2 bytes |

| Client Feature Capability | Max Video Frame Rate | Min Video Frame Rate | Min Sub-frame Rate | Audio Buffer Depth | Audio Channel Capability | Audio Sample Rate Capability |
|---|---|---|---|---|---|---|
| 4 bytes | 1 byte | 1 byte | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| Audio Sample Resolution | Mic Sample Resolution | Mic Sample Rate Capability | Keyboard Data Format | Pointing Device Data Format | Content Protection Type | Mfr Name |
|---|---|---|---|---|---|---|
| 1 byte | 1 byte | 2 bytes | 1 byte | 1byte | 2 bytes | 2 bytes |

| Product Code | Reversed 3 | Serial Number | Week of Mfr | Year of Mfr | CRC |
|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 4 bytes | 1 byte | 1 byte | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 66

cClient ID: set to zero

Protocol Version: set to 0002h

Min Protocol Version: specify the minimum protocol version (0001h)

Pre-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

Interface Type Capability: Client can function in Type 2 (2-bit) mode on the forward link (01h)

Number of Alt Displays: set to zero

Post-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

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Bitmap Width: specify the width of the bitmap (1E0h)

Bitmap Height: specify the height of the bitmap (320h)

Display Window Width: specify the width of the display window (1E0h)

Display Window Height: specify the height of the display window (320h)

Color Map Size: set to zero

Color Map RGB Width: set to zero

RGB Capability: specify the resolution of RGB format (0888h)

Monochrome Capability: set to zero

Reserved 1: set to zero

Y Cb Cr Capability: set to zero

Bayer Capability: set to zero

Reserved 2: set to zero

Client Feature Capability Indicators: 00CC8000h

Maximum Video Frame Rate Capability: specify the maximum video frame (3Ch)

Minimum Video Frame Rate Capability: specify the minimum video frame (3Ch)

Minimum Sub-frame Rate: specify the minimum sub-frame rate (00h)

Audio Buffer Depth: set to zero

Audio Channel Capability: set to zero

Audio Sample Rate Capability: Set to zero

Audio Sample Resolution: set to zero

Mic Audio Sample Resolution: set to zero

Mic Sample Rate Capability: set to zero

Keyboard Data Format: set to zero

Pointing Device Data Format: set to zero

Content Protection Type: set to zero

Mfr Name: set to 0000h

Product Code: set to 6812h

Reserved 3: set to zero

Serial Number: set to zero

Week of Manufacture: set to zero

Year of Manufacture: 00h

CRC: error check

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**Client Request and Status Packet**

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Client Request and Status Packet

| Packet Length | Packet Type=70 | cClient ID | Reverse Link Request | CRC Error Count | Client Status | Client Busy Flags | CRC |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 1 byte | 1 byte | 2 bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 70

cClient ID: set to zero

Reverse Link Request: specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.

CRC Error Count: count the number of CRC errors occurred

Client Status:

- Bit 0 – 1: capability has changed
  0: capability has not changed
- Bit 1 – indicates the client has detected an error
- Bit [7:2] – set to zero

Client Busy Flags:

- Bit 0 – bitmap block transfer function is busy
- Bit 1 – bitmap area fill function is busy
- Bit 2 – bitmap pattern fill function is busy
- Bit 3 – the graphics subsystem is busy
- Bit [15:4] – set to zero

CRC: error check

**Register Access Packet**

Register Access Packet is utilized when setting instruction to the RM68120. This packet cannot be used for RAM access.

Register Access Packet

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| Packet Length | Packet Type=146 | bClient ID | Read/Write Info | Register Address | Parameter CRC | Register Data List | Register Data CRC |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 4 bytes | 2 bytes | (Packet Length -14) bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 146

bClient ID: set to zero

Read/Write Info:

| Bits[15:14] | Read/Write Flags |
|---|---|
| 00 | Write |
| 01 | Reserved |
| 10 | Read |
| 11 | Response to read |

Bit [13:0] – specifies the number of 32-bit register data list items to be transferred in the Register Data List Filed.

Register Address: upper bits shall set to zero

Parameter CRC: error check from packet length to the register address

Register Data List: written (or read) registers to (from) client

Register Data CRC: error check of the register data list

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**Video Stream Packet**

The RM68120 supports the Video Stream Packet to transfer display data including RGB data to RAM.

Video Stream Packet

| Packet Length | Packet Type=16 | bClient ID | Video Data Format Desriptor | Pixel Data Attributes | X Left Edge | Y Top Edge |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| X Right Edge | Y Bottom Edge | X Start | Y Start | Pixel Count | Parameter CRC | Pixel Data | Pixel Data CRC |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | (Packet Length -26) bytes | 2 bytes |

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Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 16

bClient ID: set to zero

Video Data Format Descriptor

| [15:12] | [11:18] | [7:4] | [3:0] | Transfer pixel format |
|---|---|---|---|---|
| 0101 | 0x8 | 0x8 | 0x8 | Packed 24 bits pixel RGB format (R:G:B=8:8:8) |
| 0101 | 0x6 | 0x6 | 0x6 | Packed 18 bits pixel RGB format (R:G:B=6:6:6) |
| 0101 | 0x5 | 0x6 | 0x5 | Packed 16 bits pixel RGB format (R:G:B=5:6:5) |
| Others setting disabled | | | | |

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68120 (00C3h)

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Pixel Data Format

| MDDI data byte | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Color |
|---|---|---|---|---|---|---|---|---|---|---|
| RGB 5:6:5 | Byte n | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | 65-Color (1 pixel/ 16 bits RGB format) |
| | Byte n+1 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | |
| RGB 6:6:6 | Byte n | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | 262K-Color (1 pixel/ 18 bits RGB format) |
| | Byte n+1 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | |
| | Byte n+2 | B5 | B4 | B3 | B2 | B1 | B0 | R5 | R4 | |
| RGB 8:8:8 | Byte n | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 16.7M-Color (1 pixel/ 24 bits RGB format) |
| | Byte n+1 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | |
| | Byte n+2 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | |

**Flexible Video Stream Packet**

The RM68120 supports the Flexible Video Stream Packet to transfer display data including RGB data to RAM. This allows for a reduction in the number of fields sent in an environment where one or more fields are

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not changing values.

Flexible Video Stream Packet

| Packet Length | Packet Type=20 | bClient ID | Field Present Flags | Video Data Format Description | Pixel Data Attributes | X Left Edge | Y Top Edge |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| X Right Edge | Y Bottom Edge | X Start | Y Start | Pixel Count | Parameter CRC | Pixel Data | Pixel Data CRC |
|---|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | Packet Length – present header bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 20

bClient ID: set to zero

Field Present Flags: indicates the field in the packet is present (value “1”) or not present (value “0”).

- Bit 0: indicates the presence of the Video Data Format Description Field.
- Bit 1: indicates the presence of the Pixel Data Attributes Field.
- Bit 2: indicates the presence of the X Left Edge Field.
- Bit 3: indicates the presence of the Y Top Edge Field.
- Bit 4: indicates the presence of the X Right Edge Field.
- Bit 5: indicates the presence of the Y Bottom Edge Field.
- Bit 6: indicates the presence of the X Start Field.
- Bit 7: indicates the presence of the Y Start Field.
- Bit 8: indicates the presence of the Pixel Count Field.
- Bits [15:9] are all “0”.

Video Data Format Descriptor

| [15:12] | [11:18] | [7:4] | [3:0] | Transfer pixel format |
|---|---|---|---|---|
| 0101 | 0x8 | 0x8 | 0x8 | Packed 24 bits pixel RGB format (R:G:B=8:8:8) |
| 0101 | 0x6 | 0x6 | 0x6 | Packed 18 bits pixel RGB format (R:G:B=6:6:6) |
| 0101 | 0x5 | 0x6 | 0x5 | Packed 16 bits pixel RGB format (R:G:B=5:6:5) |
| Others setting disabled | | | | |

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

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X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68120 (00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

**Windowless Video Stream Packet**

The RM68120 supports the Windowless Video Stream Packet to transfer display data including RGB data to RAM. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information.

Windowless Video Stream Packet

| Packet Length | Packet Type=22 | bClient ID | Video Data Format Description | Pixel Data Attributes | Pixel Count | Parameter CRC |
|---|---|---|---|---|---|---|
| 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes | 2 bytes |

| Pixel Data | Pixel Data CRC |
|---|---|
| Packet Length – 14 bytes | 2 bytes |

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 22

bClient ID: set to zero

Video Data Format Descriptor

| [15:12] | [11:18] | [7:4] | [3:0] | Transfer pixel format |
|---|---|---|---|---|
| 0101 | 0x8 | 0x8 | 0x8 | Packed 24 bits pixel RGB format (R:G:B=8:8:8) |
| 0101 | 0x6 | 0x6 | 0x6 | Packed 18 bits pixel RGB format (R:G:B=6:6:6) |
| 0101 | 0x5 | 0x6 | 0x5 | Packed 16 bits pixel RGB format (R:G:B=5:6:5) |
| Others setting disabled | | | | |

Pixel Data Attributes: The pixel data is written to RAM buffer of RM68120 (00C3h)

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Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

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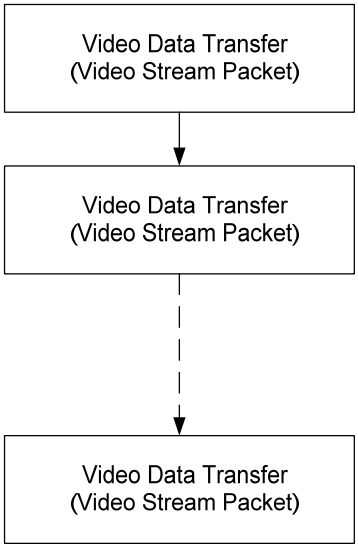
### 7.7.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.




Writing Video Data to Memory Sequence

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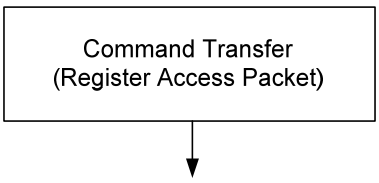
### 7.7.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.

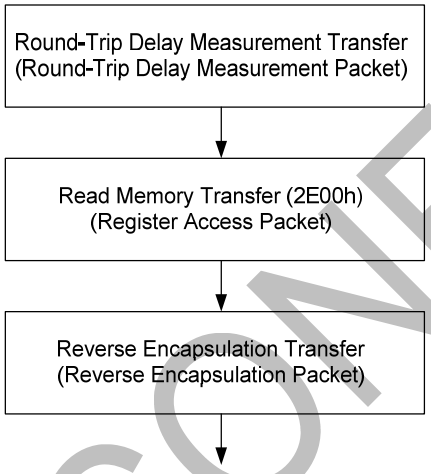
Writing Register Sequence:




### 7.7.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2E00h) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Video Data from Memory Sequence:




Notes:

1. X addresses for memory data read is set by 2A00h and 2A01h (XS[15:0]).

The parameters of 2A00h and 2A01h are stored on relative registers while command 2A00h~2A03h are executed completely. See also section “6.1 User Command Set” and Note 2.

2. Y addresses for memory data read is set by 2B00h and 2B01h (YS[15:0]).

The parameters of 2B00h and 2B01h are stored on relative registers while command 2B00h~2B03h are executed completely. See also section “6.1 User Command Set” and Note 2.

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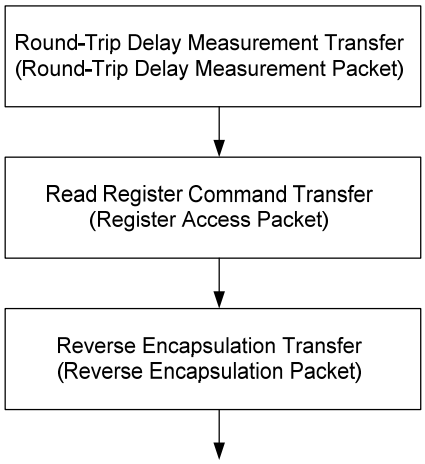
### 7.7.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Register Sequence:

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### 7.7.7 Hibernation Setting

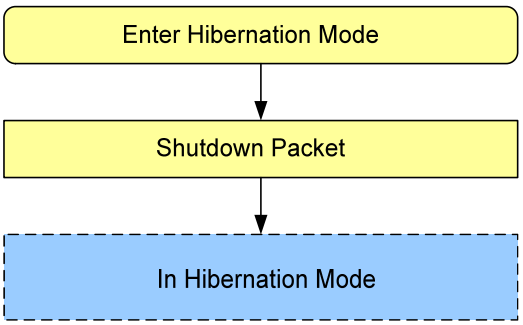
The Client MDDI of the RM68120 provides a hibernation setting. The methods for waking up the hibernation mode can be determined based on actual usage.

| Wake-up | Condition |
|---|---|
| Host-Initiated Wake-up | Wake up the MDDI link by MDDI Host |

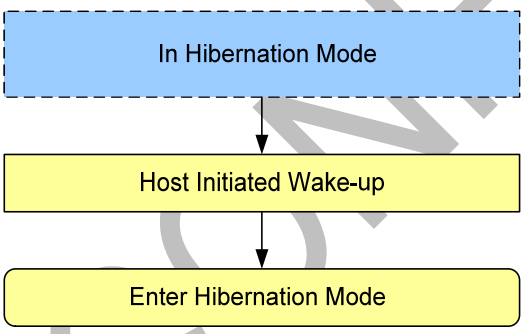
Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained.

Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

**Hibernation setting sequence**




**Hibernation Wake-up sequence**

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### 7.7.8 MDDI Deep Standby Mode Setting

The Client MDDI of the RM68120 includes a MDDI deep standby mode setting so it can enter a off state and reduce power consumption during Hibernation mode.

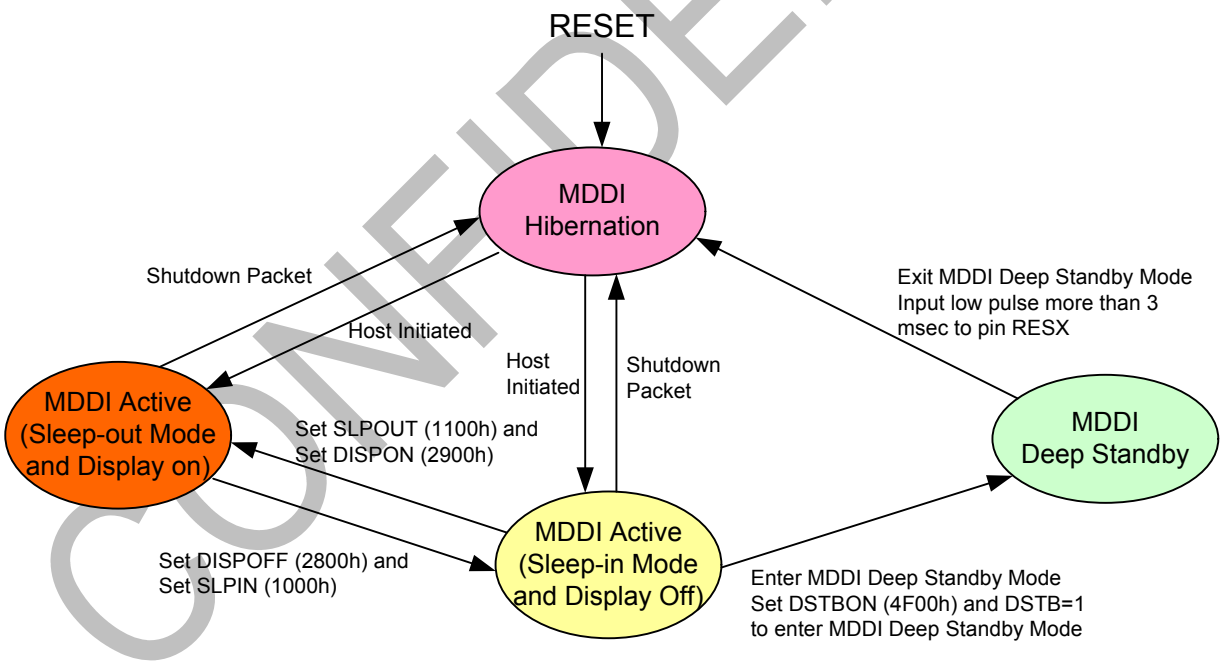
The MDDI enters Hibernation mode when a Shutdown Packet is sent. The standby power needs of the Client MDDI can be reduced, even while the MDDI Link is maintained in Hibernation mode.

When entering MDDI deep standby mode, the RM68120 stops operation rather than maintaining Hibernation mode. Input low pulse 3 msec from RESX pin to cancel deep standby mode, after which a Host-Initiated Wake-up should cancel the Hibernation mode.

When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

Follow the sequence indicated in the VESA MDDI specifications when initiating or canceling the Hibernation mode.

State Transitions in MDDI Deep Standby Mode:




Note: When the RM68120 is in the MDDI Hibernation mode or MDDI deep standby mode, both links are in the link hibernation states.

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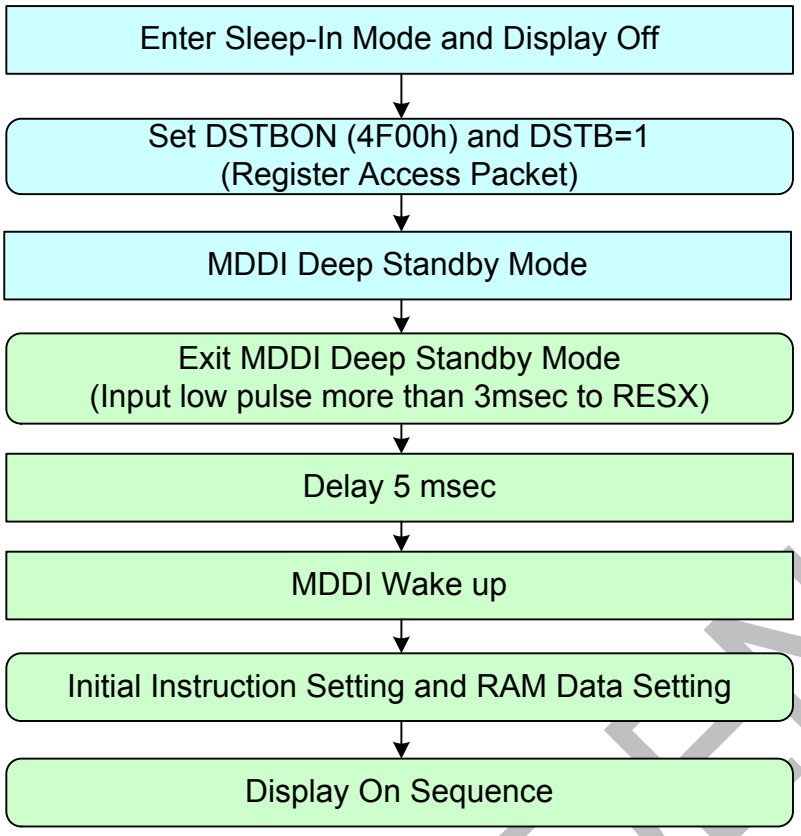
**MDDI Deep Standby Mode Sequence**




Note: When in MDDI Deep Standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

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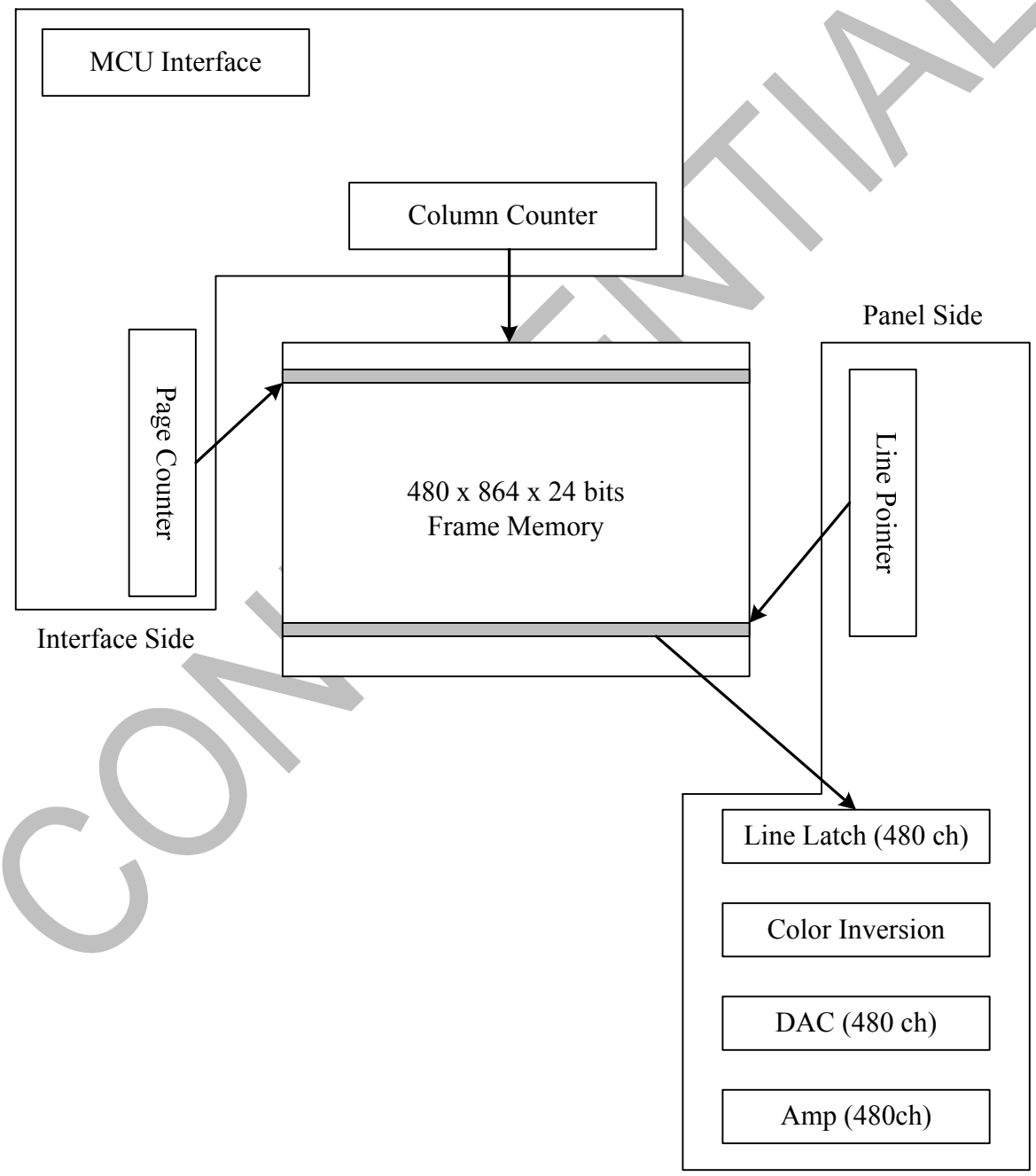
### 7.8 Display Data RAM

#### 7.8.1 Configuration

The display data RAM stores display dots and consists of 9,953,280bits (480 x 24 x 864 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.

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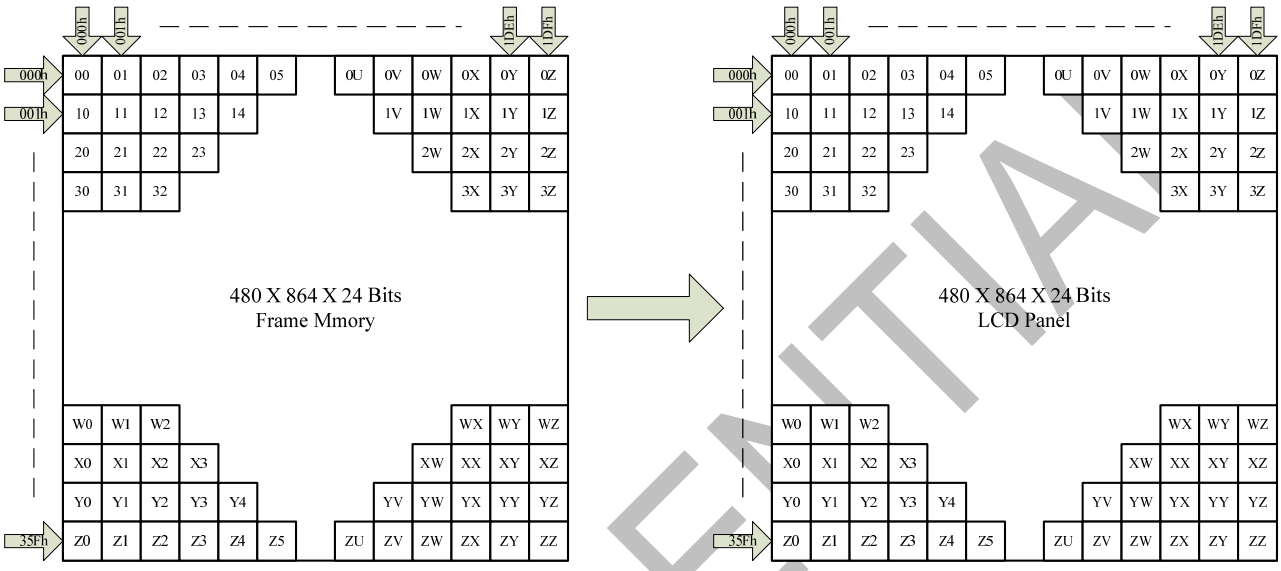
### 7.8.2 Memory to Display Address Mapping

In this mode, content of the frame memory within an area where column pointer is 0000h to 01DFh and page pointer 0000h to 035Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

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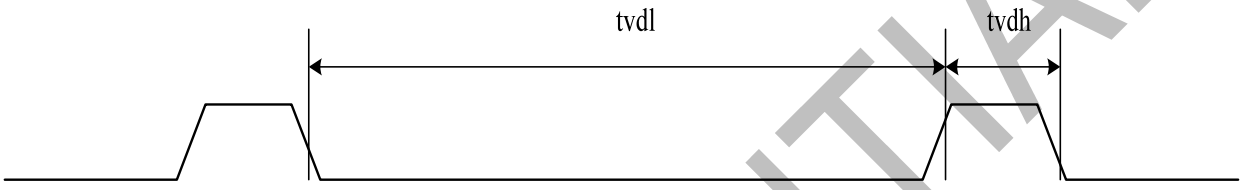
### 7.9 Tearing Effect Output

The tearing effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

#### 7.9.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:

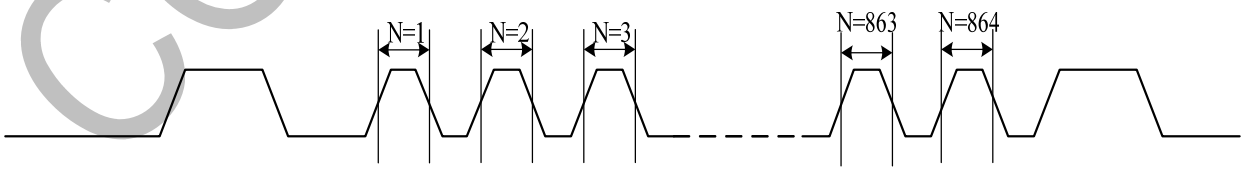



tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

Mode 2, the tearing effect output signal consist of V-sync and H-sync information:

thdh = The LCD display is not updated from the frame memory.
thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.




N = The N-th scanning line which set by register N[15:0] of command STESL(44h).

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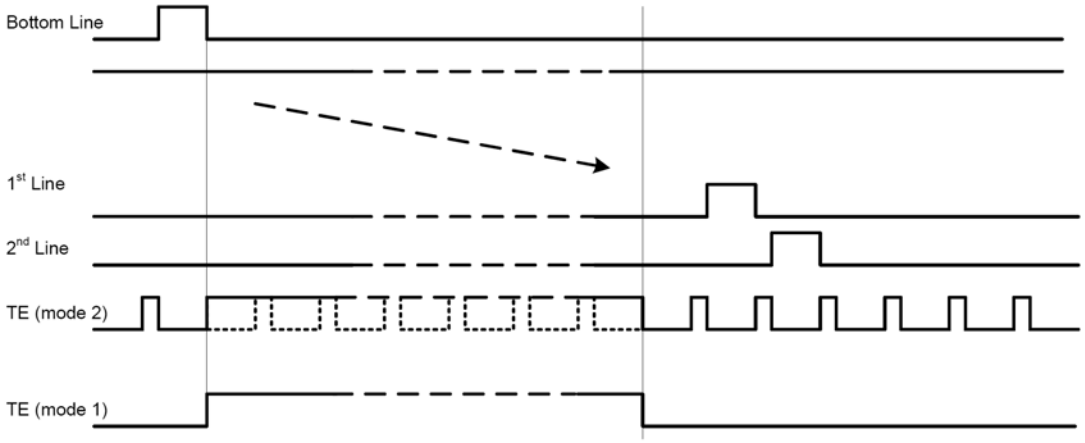


Note. During Sleep In mode, the tearing effect output signal is active low.

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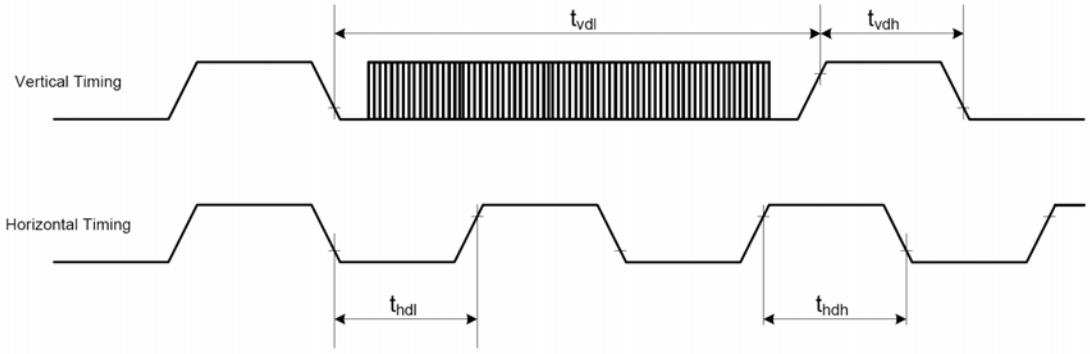
### 7.9.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

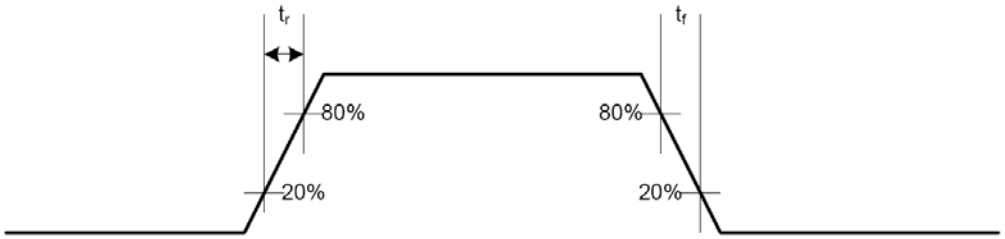



AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

| Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|
| tvdl | Vertical timing low duration | TBD | | ms | |
| tvdh | Vertical timing high duration | TBD | | us | |
| thdl | Horizontal timing low duration | TBD | | us | |
| thdh | Horizontal timing high duration | TBD | | us | |

Notes:

1. The timings apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.




The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

| TEON (35h) | TELOM (35h, 1st bit) | TE signal Output |
|---|---|---|
| 0 | * | GND |
| 1 | 0 | TE (Mode 1) |
| 1 | 1 | TE (Mode 2) |

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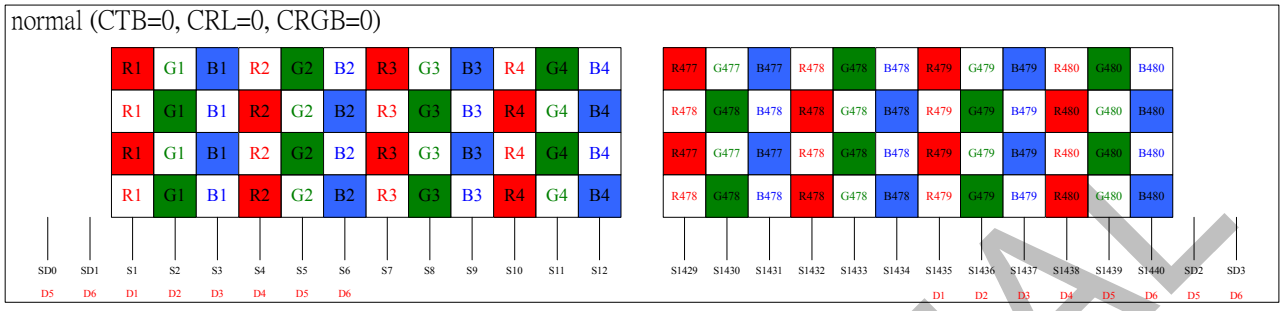
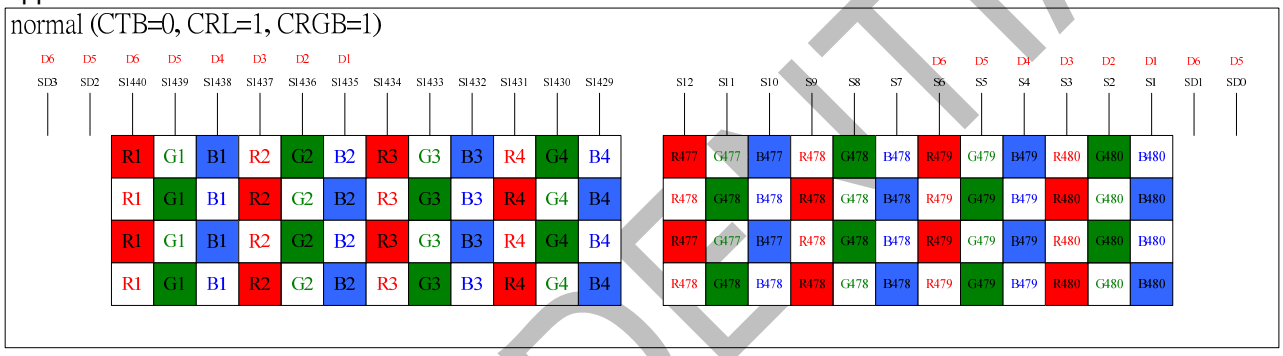
## 7.10 Panel Type

### 7.10.1 Normal Type

Bottom Side

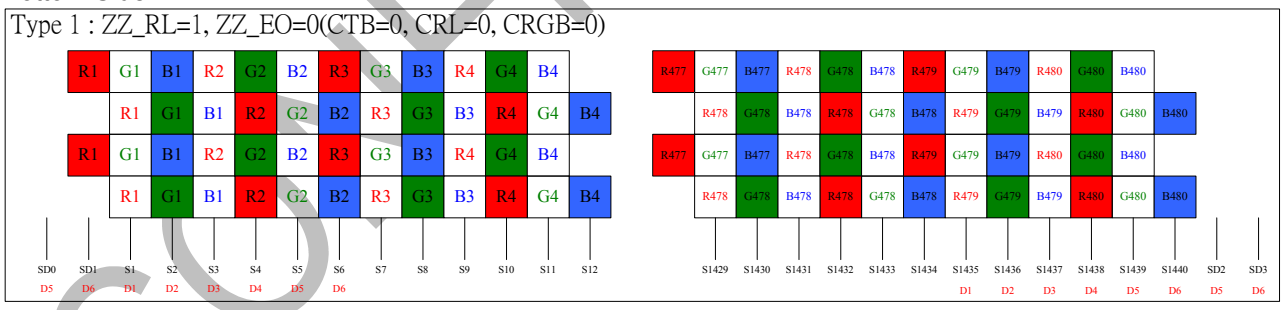



Upper Side

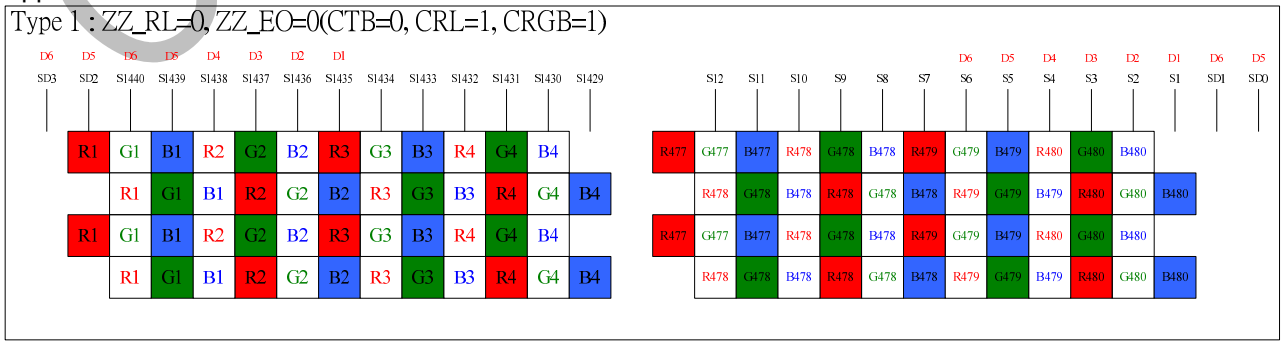



### 7.10.2 Zigzag Type 1

Bottom Side




Upper Side

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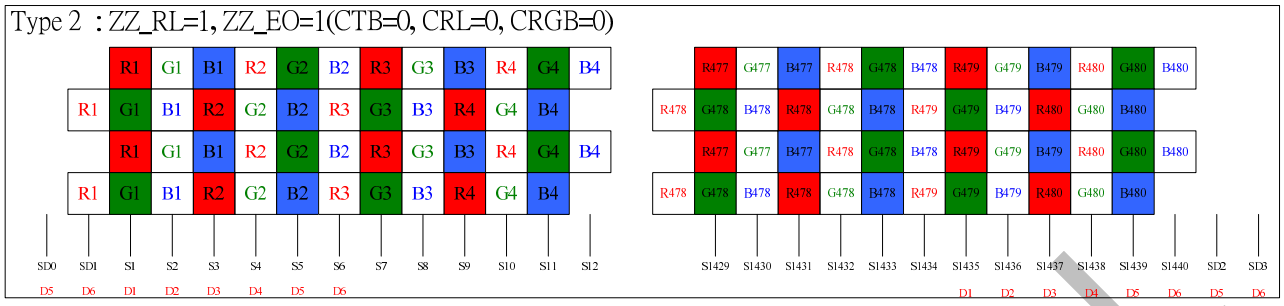
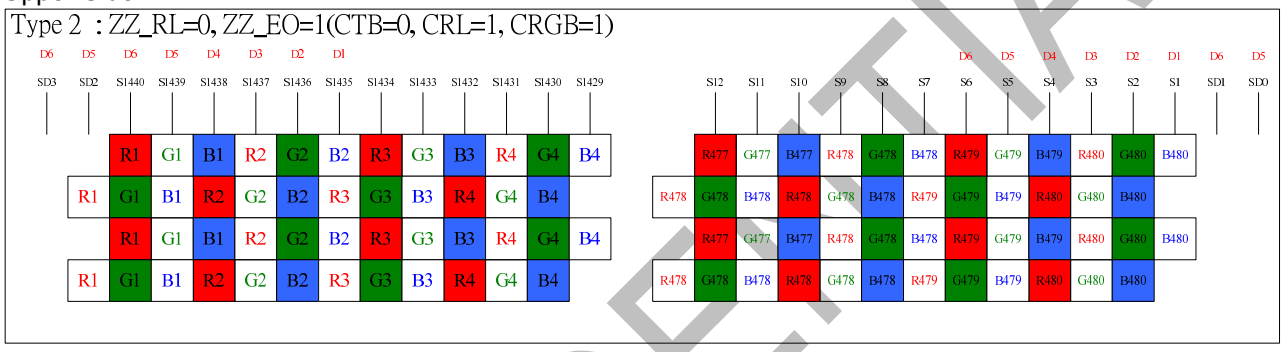
### 7.10.3 Zigzag Type 2

Bottom Side

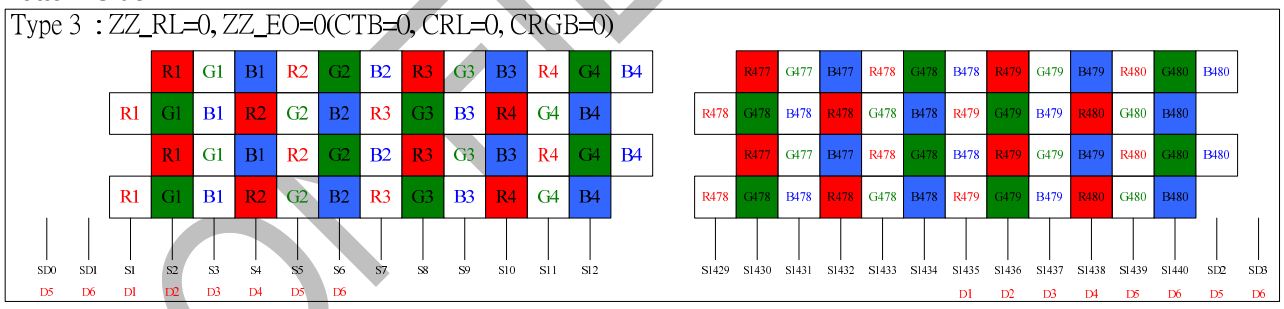



Upper Side

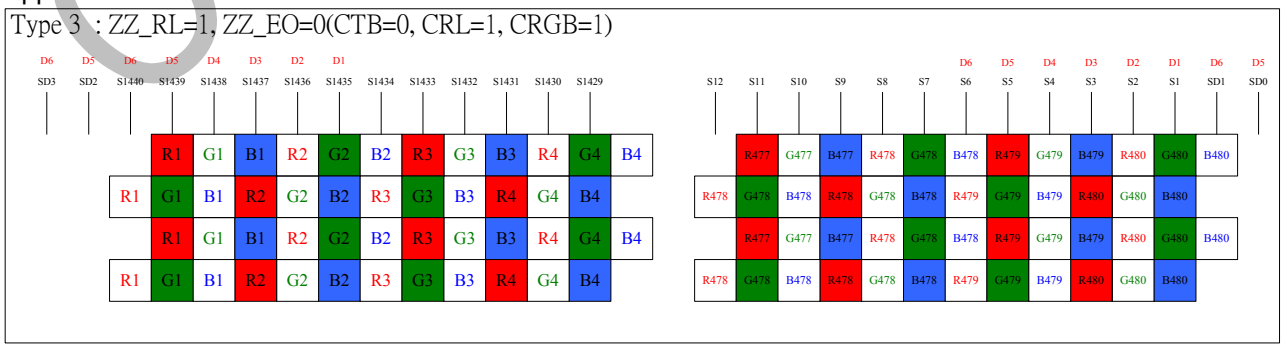



### 7.10.4 Zigzag Type 3

Bottom Side




Upper Side

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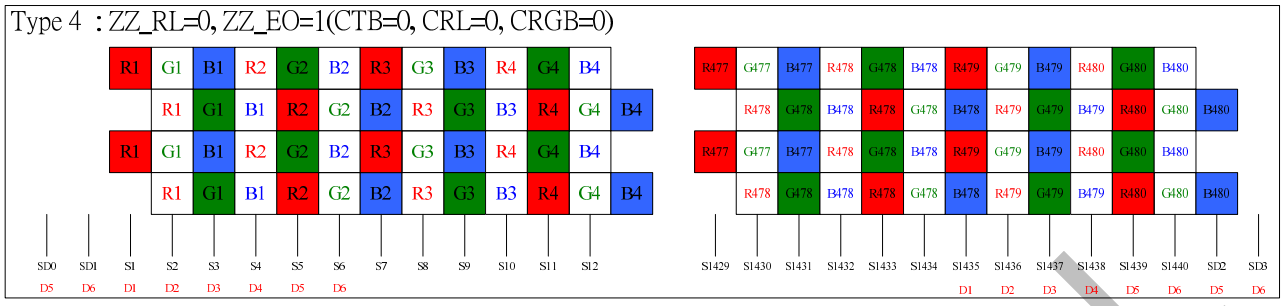
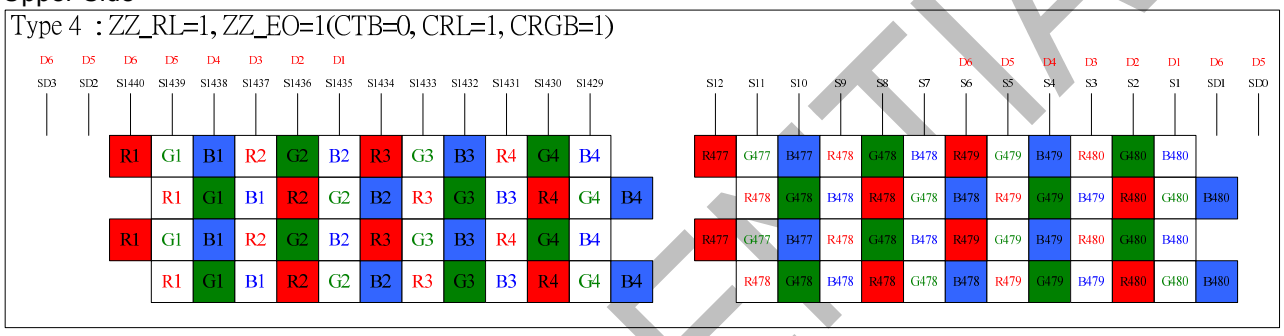
### 7.10.5 ZigZag Type 4

Bottom Side




Upper Side

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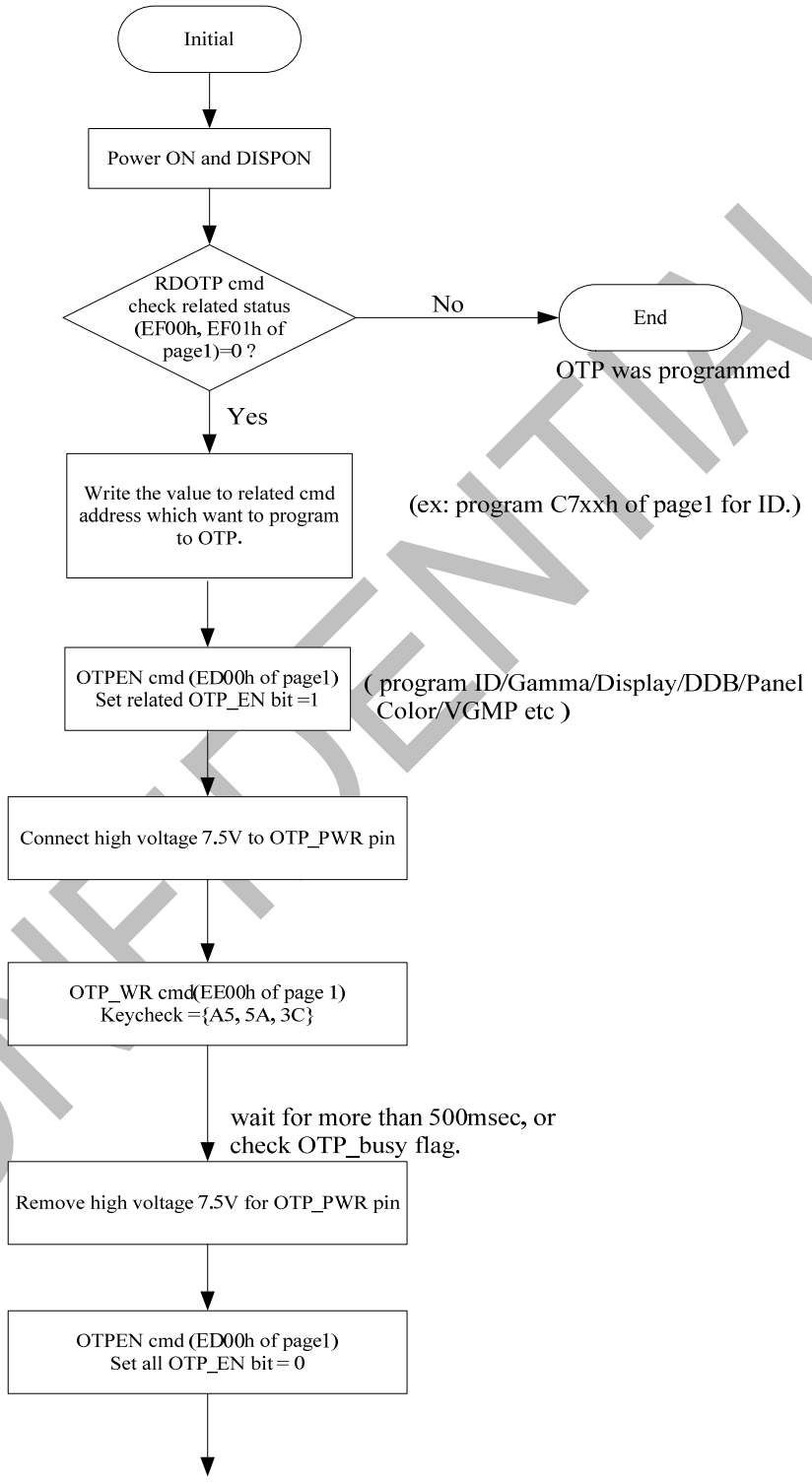
### 7.11 OTP Porgram Sequence




OTP Programming Flow

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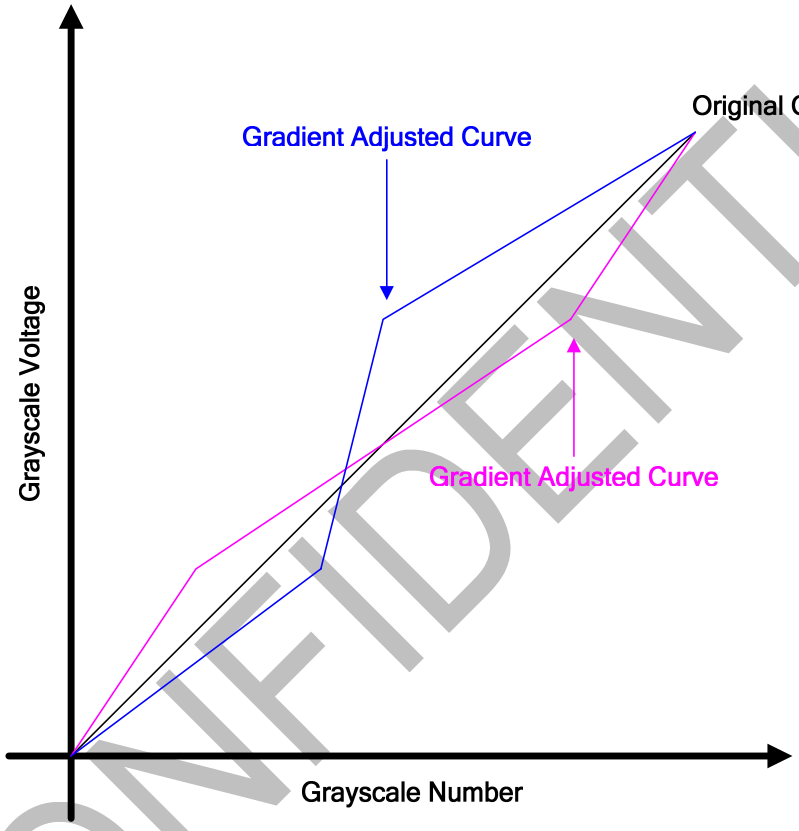
### 7.12 Independent Gamma Correction Function

The RM68120 supports indenpedent gamma adjustment function for R color, G color and B color to display in 16.7M colors. The function is performed by determining grayscale levels that use gamma adjustment registers. The RM68120 also provides gradient control registers for adjustments of gamma curve.

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### 7.13 Dynamic Backlight Control

The function of Dynamic Display Backlight is used to reduce the power consumption of display backlight. It includes Content Adaptive Brightness Control (CABC) and Light-Sensor Automatic Brightness Control (LABC) functions. Both two functions are used to generate a proper PWM signal according to display image and ambient light information. User could apply this PWM signal to control other device(s) (Such as power IC or LED driver IC). When the CABC and LABC functions are enabled and cooperate with external circuits (such as LED driver circuit), the power consumption of backlight will be reduced with keeping acceptable display quality.

The CABC function is used to reduce the power consumption of display backlight. Contents adaptation means that the grayscale level of image contents is raised while lowering brightness of the backlight simultaneously to keep same perceived brightness. The adjustment of grayscale level and brightness reduction is based on the display image contents. Thus the power consumption reduction depends on the contents of the image. The display image and brightness are dynamically processed by CABC block.

In order to achieve a better display quality and reduce power consumption of the backlight at the same time, there are 3 different modes, user interface image mode, still picture mode and moving image mode, for user selections.

The LABC function combines several mechanisms to provide a smooth control of sensed light information. Flicker Removal is used to eliminate external light source flicker (e.g. 50 and 60 Hz). Hysteresis is used for preventing the transient variation of luminance. When the LABC function is enabled, the information of the ambient light is sent to the brightness control block. The user can read ambient light information or this information can be used for automatic brightness control by the brightness control block. It is also possible to control the brightness manually.

With combination of the CABC and the LABC processed results, the display output brightness is adjusted.

Display Backlight Brightness = LABC Brightness Ratio (or Manual Setting Ratio) x CABC Brightness Ratio

The function of CABC affects both display brightness ratio and grayscale level. The function of LABC affects display brightness ratio only.

Display Brightness Output of combinations of CABC and LABC function

| | LABC(Manual) Brightness Ratio | CABC(Manual) Brightness Ratio | Calculation Ratio | Brightness Output of LEDPWM | Image Status |
|---|---|---|---|---|---|
| **Case 1** | 70% | 60% | 42% | 42% | CABC modified |
| **Case 2** | 50% | 100% | 50% | 50% | CABC modified |
| **Case 3** | 40% | 30% | 12% | 12% | CABC modified |

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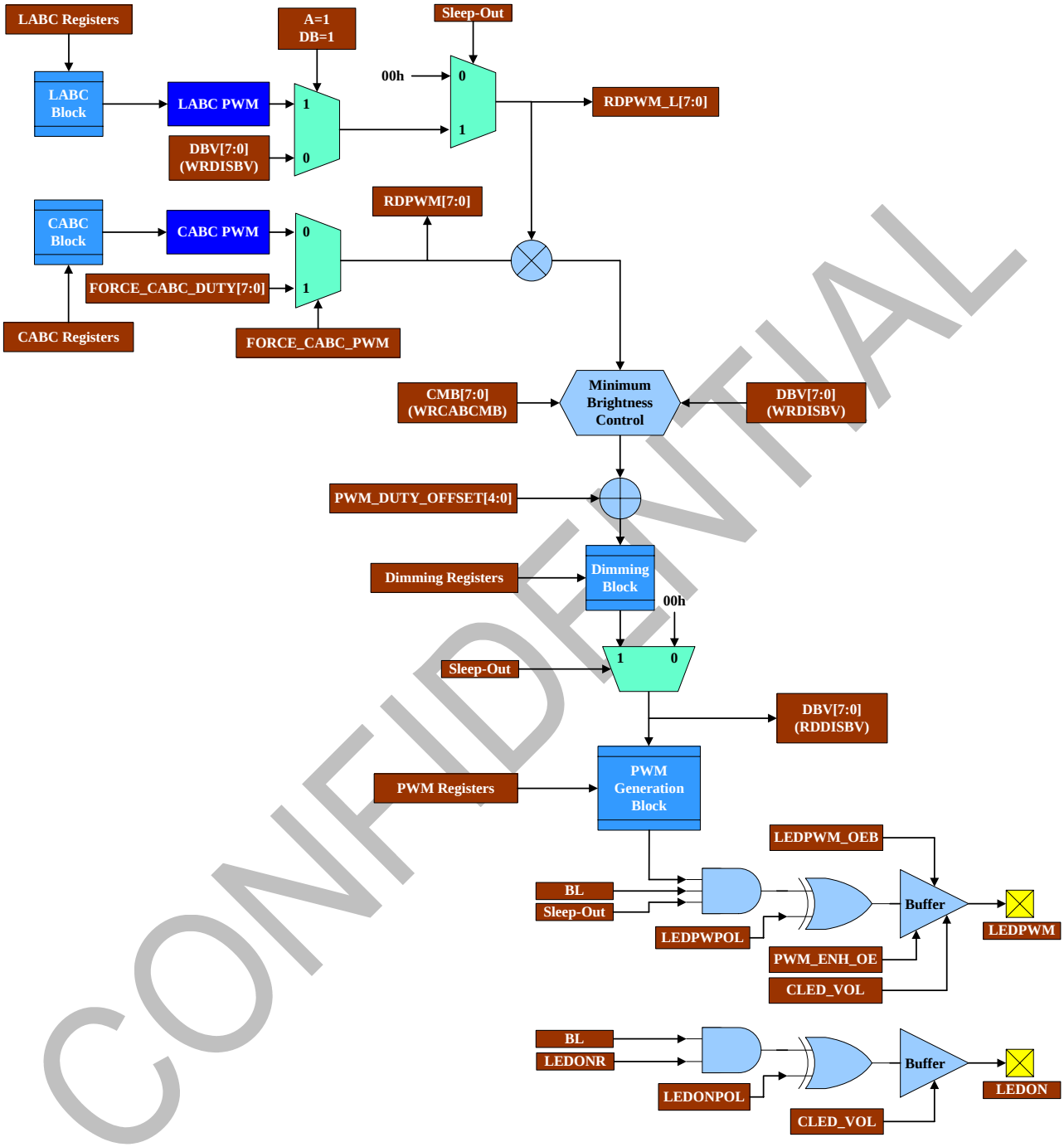
### 7.13.1 PWM Control Architecture




**Internal Display Backlight Control**

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The register bit “BL” is used to turn on or turn off backlight control lines, “LEDPWM” pin and “LEDON” pin. Normally, if user want to disable the display backlight completely and immediately, user can set “BL = 0”. Relations between “BL” and control lines are list below.

| BL | LEDPWPOL | Status of LEDPWM Pin |
|---|---|---|
| 0 | 0 | 0 |
| | 1 | 1 |
| 1 | 0 | Original polarity of PWM signal |
| | 1 | Inversed polarity of PWM signal |

| BL | LEDONPOL | Status of LEDON Pin |
|---|---|---|
| 0 | 0 | 0 |
| | 1 | 1 |
| 1 | 0 | LEDONR |
| | 1 | Inverted LEDONR |

The register bit “BCTRL” is used to turn on or turn off backlight control block. Display brightness which is controlled by LEDPWM will be turn off when user set “BCTRL = 0”.

| BCTRL | Value of DBV[7:0] (RDDISBV) | Display Backlight Status |
|---|---|---|
| **0** | 00h | off |
| **1** | Determined by CABC and LABC | on |

The register bit “PWM_ENH_OE” is used to adjust the driving ability of “LEDPWM” pin (“PWM_ENH_OE” can not affect the driving ability of “LEDON” pin).

The register bit “CLED_VOL” is used to choose different output logical voltage level for LEDON, LEDPWM pins. This bit is valid when:

(1) DSTB_DEL=low, or (2) DSTB_SEL=high, VDDI=1.65~3.3V and VSEL=high

(The output level is VSSI to DIOPWR for other VDDI and VSEL conditions in DSTB_SEL=high). See below for the selection output level

| CLED_VOL | LEDON/LEDPWM Output Level |
|---|---|
| 0 | VSSI to VDDI |
| 1 | VSSI to VDDA |

| PWM_ENH_OE | Driving Ability of LEDPWM Pin |
|---|---|
| 0 | 1X driving ability of LEDPWM |
| 1 | 2X driving ability of LEDPWM |

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The register bit “A” is used to enable / disable LABC functions. Sampling of ambient light information started after setting the register bit “A”. User has to write the ambient light information into the register “LS[15:0]” via system interface.

The register bit “DB” is used to select manual or automatic brightness control. When “DB=0”, the display backlight brightness can be affected by setting register “DBV[7:0] “ (WRDISBV) manually. When “DB =1” display backlight is affected by automatic brightness control. Relations between register bits “DB”, “A”, DBV[7:0] (WRDISBV), RDPWM[7:0], and RDPWM_L[7:0] are listed in below tables.

| Driver IC State | A | DB | Display Backlight Control |
|---|---|---|---|
| **Sleep-In** | x | x | Disable |
| **Sleep-Out** | 0 | 0 | Control by manual setting DBV[7:0] (WRDISBV) |
| **Sleep-Out** | 0 | 1 | Control by manual setting DBV[7:0] (WRDISBV) |
| **Sleep-Out** | 1 | 0 | Control by manual setting DBV[7:0] (WRDISBV) |
| **Sleep-Out** | 1 | 1 | Control by LABC function |

**“FORCE_CABC_PWM=0”, “CMB[7:0] = 00h” (WRCABCMB), “PWM_DUTY_OFFSET[4:0]=00h”, “BL=1”, “BCTRL=1”, Sleep-Out Mode**

| CABC Status | A | DB | RDPWM_L[7:0] | RDPWM[7:0] | Display Backlight Brightness |
|---|---|---|---|---|---|
| **Off Mode** | 0 | 0 | Determined by DBV[7:0] (WRDISBV) | FFh | Determined by DBV[7:0] (WRDISBV) |
| | 0 | 1 | | | |
| | 1 | 0 | | | |
| | 1 | 1 | Determined by LABC Function | FFh | Determined by LABC Function |
| **UI-Mode / Still-Mode / Moving-Mode** | 0 | 0 | Determined by DBV[7:0] (WRDISBV) | Determined by CABC Function | Determined by DBV[7:0] (WRDISBV) x CABC Function |
| | 0 | 1 | | | |
| | 1 | 0 | | | |
| | 1 | 1 | Determined by LABC Function | Determined by CABC Function | Determined by LABC Function x CABC Function |

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The writing register DBV[7:0] (WRDISBV) is used to adjust the backlight brightness value manually when LABC function is disabled (register bit “A=0” and “DB=0”). Note that reading register DBV[7:0] (RDDISBV) is used to indicate the output PWM signal duty variation. That means DBV[7:0] (RDDISBV) is also affected by CABC function when CABC function is enable.

The register setting CMB[7:0] (WRCABCCMB) is used to limit the minimum PWM duty in order to prevent the backlight brightness from being too dark.

The register FORCE_CABC_DUTY[7:0] is used to perform a fixed PWM duty of CABC output when the register bit “FORCE_CABC_PWM=1”.

The register bit “DD” is used to enable or disable the dimming function for LABC / Manual Brightness Control. Smooth transition of PWM duty is performed when “DD=1”. Dimming function is applied only when driver IC is in sleep-out status. CABC function and LABC function are available only when driver IC is in sleep-out status. Availability of functions is listed in below table.

| Driver IC Status | CABC Function | LABC Function | Dimming Function | Display Backlight Status |
|---|---|---|---|---|
| **Sleep-In** | Not Available | Not Available | Not Available | Turn-Off |
| **Sleep-Out** | Available | Available | Available | Controllable |

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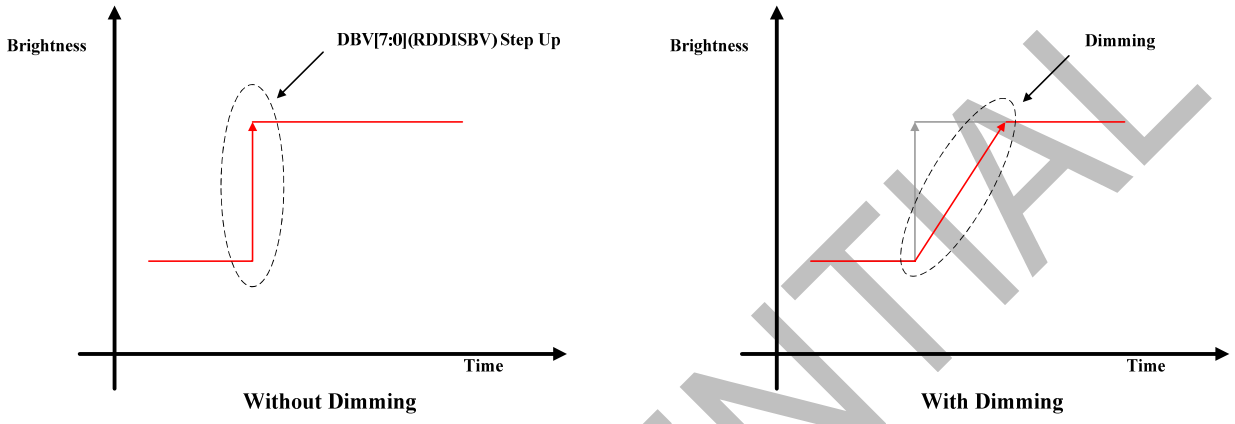
### 7.13.2 Dimming Function for LABC and Manual Brightness Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. The dimming function curves for LABC and Manual Brightness Control can be configured the same or not the same in increment and decrement directions. The basic idea is described below.




Basic Concept of Dimming Function

The RM68120 provides two types of PWM duty dimming mechanism, “Fixed-Time Dimming” and “Fixed-Slope Dimming”, for LABC and manual brightness control. The setting of dimming types for rising dimming and falling dimming is independent. The register bit “SEL_IN” is for rising dimming (increment dimming), and the register bit “SEL_DE” is for falling dimming (decrement dimming).

| SEL_IN | SEL_DE | Rising Dimming Type | Falling Dimming Type |
|---|---|---|---|
| 0 | 0 | Fixed-Time Dimming | Fixed-Time Dimming |
| 0 | 1 | Fixed-Time Dimming | Fixed-Slope Dimming |
| 1 | 0 | Fixed-Slope Dimming | Fixed-Time Dimming |
| 1 | 1 | Fixed-Slope Dimming | Fixed-Slope Dimming |

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**Fixed-Time Dimming Type**

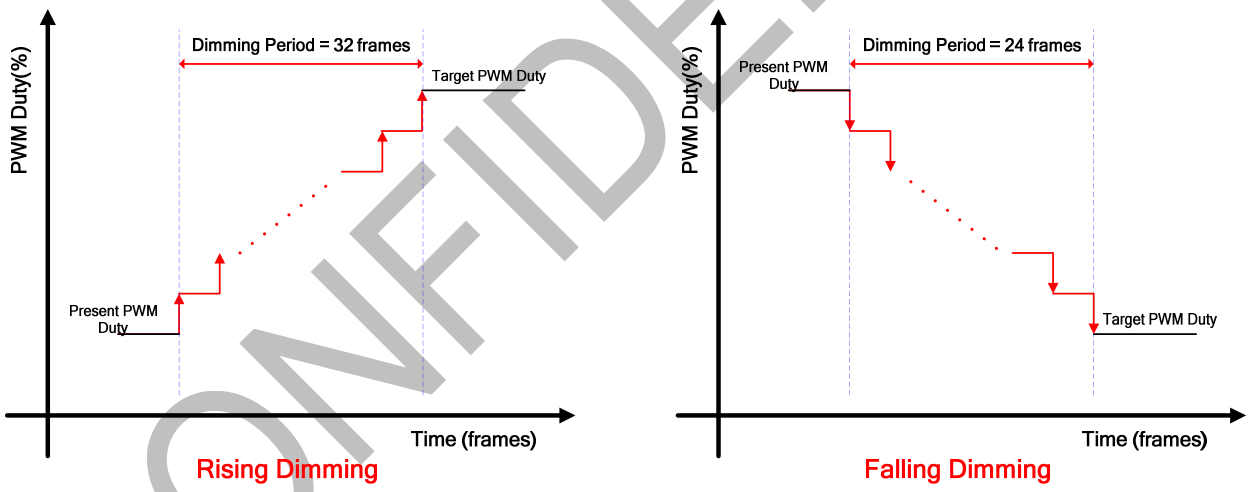
The total dimming steps and can be set by registers “DMSTP_L[2:0]”, “DM_IN[3:0]”, and “DM_DE[3:0]”, respectively. These three registers can determine the total dimming time.

The unit of registers “DM_IN[3:0]” and “DM_DE[3:0]” is “frame(s) per step”. The unit of register DMSTP_L[2:0] is “step(s)”

**For Example:**

| Register Name | Value | Description |
|---|---|---|
| **SEL_IN** | 0 | Fixed-Time dimming for rising dimming |
| **SEL_DE** | 0 | Fixed-Time dimming for falling dimming |
| **DM_IN[3:0]** | 7h | 8 frames time for each step |
| **DN_DE[3:0]** | 5h | 6 frames time for each step |
| **DMSTP_L[2:0]** | 1h | dimming steps is 4 steps |

Total dimming time of “rising dimming” is 32-frames time length (8 frames x 4).
Total dimming time of “falling dimming” is 24-frames time length (6 frames x 4).

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**Fixed-Slope Dimming Type**

The increasing / decreasing PWM duty during a time period can be set by register “STEP_IN[3:0]”, “STEP_DE[3:0]”, “DM_IN[3:0]”, and “DM_DE[3:0]”, respectively. These three registers can determine some characteristics of dimming curves.

The unit of registers STEP_IN[3:0] and STEP_DE [3:0] is “duty ratio” (FFh is 100%, and 00h is 0%). The unit of register DM_IN[3:0] and DM_DE[3:0] is “frame(s) per step”.

**For Example:**

| Register Name | Value | Description |
|---|---|---|
| **SEL_IN** | 1 | Fixed-Slope dimming for rising dimming |
| **SEL_DE** | 1 | Fixed-Slope dimming for falling dimming |
| **STEP_IN[3:0]** | 8h | PWM increment is 8 for each step |
| **STEP_DN[3:0]** | 5h | PWM decrement is 5 for each step |
| **DM_IN[3:0]** | 3h | 4 frames time for each step |
| **DM_DE[3:0]** | 5h | 6 frames time for each step |

When present PWM duty is “0x64” (100 in decimal), target PWM duty is 0x14 (20 in decimal), so the total dimming steps will be:

Total dimming steps = (Present PWM Duty - Target PWM duty) / (PWM decrement)

= (100 - 20) / 5 = 16 steps

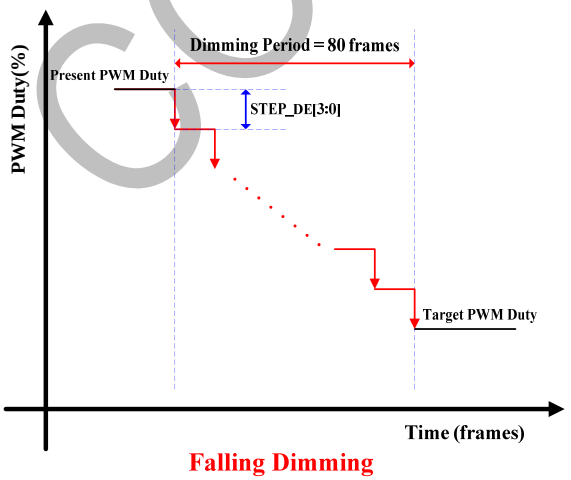
So total dimming time for falling dimming is 80 frames (16 Steps x 5)

When new target PWM duty is “0x64”, the total dimming steps will be:

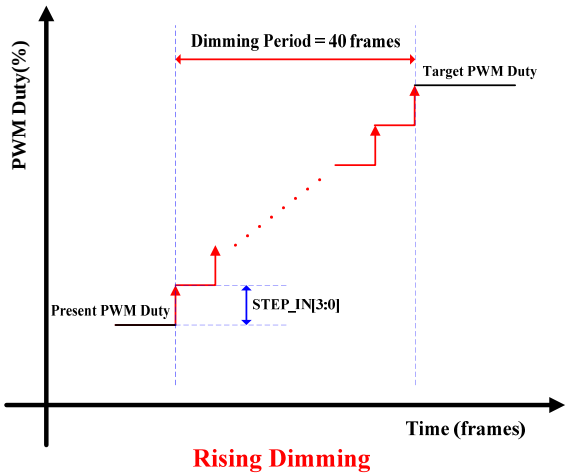
Total dimming steps = (Target PWM Duty - Present PWM duty) / (PWM increment)

= (100 - 20) / 8 = 10 steps

So total dimming time for rising dimming is 40 frames (10 Steps x 4)



Falling Dimming



Rising Dimming

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### 7.13.3 PWM Signal Setting for CABC and LABC

The registers “PWMDIV[7:0]” can change the frequency of PWM signal(LEDPWM) and the register “PWM_DUTY_OFFSET[4:0]” can perform a duty compensation of the PWM signal. The “FOSC” is used to provide clock source for the internal PWM circuit. Three PWM operation frequency can be chosen by setting register “PWMF[1:0]”, and the real PWM frequency can be quickly estimated by the bellow formula.

| PWMF[1:0] | PWM Operation Frequency ($F_{osc}$) |
|---|---|
| **00** | 7 MHz |
| **01** | 14 MHz |
| **10** | 3.5 MHz |
| **11** | (not used) |

$$PWM\ Frequency = \frac{F_{osc}}{256 \times PWMDIV[7:0]}$$

$$PWM\ Duty = \frac{DBV[7:0](RDDISBV)+1}{256}$$

**For example:**

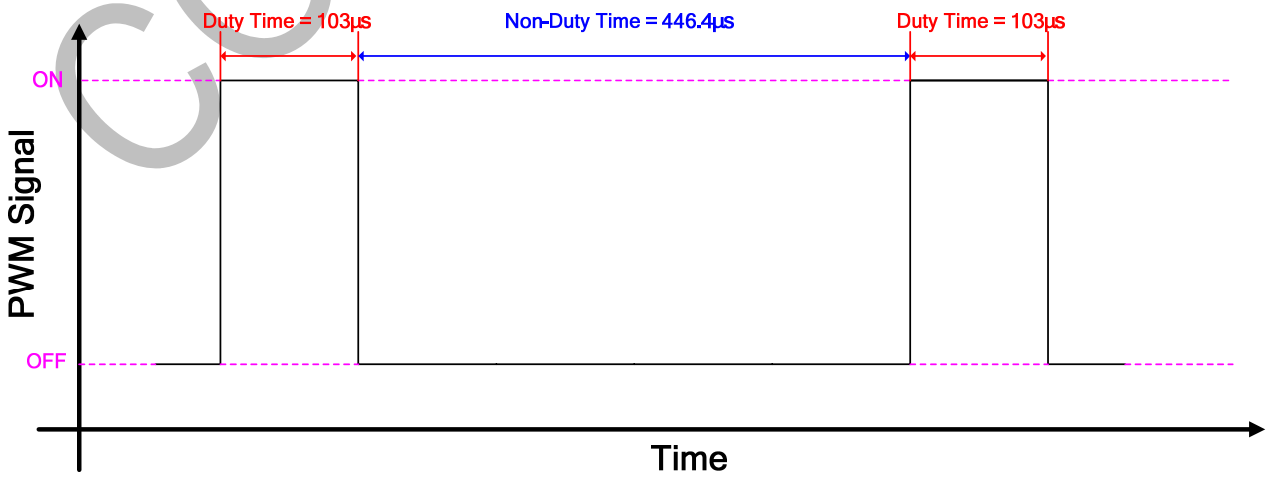
If “PWDIV[7:0]=0x0F”, “PWMF[1:0]=0x0”, “DBV[7:0]=2Fh”(RDDISBV)

$$PWM\ Frequency = \frac{7MHz}{256 \times 15} \approx 1.82KHz$$

“DBV[7:0]=2Fh” means PWM duty ratio is about 18.75%

$$PWM\ Duty\ Time = 18.75\% \times \frac{1}{1.82KHz} \approx 103.0\mu s$$

$$PWM\ non-Duty\ Time = 81.25\% \times \frac{1}{1.82KHz} \approx 446.4\mu s$$

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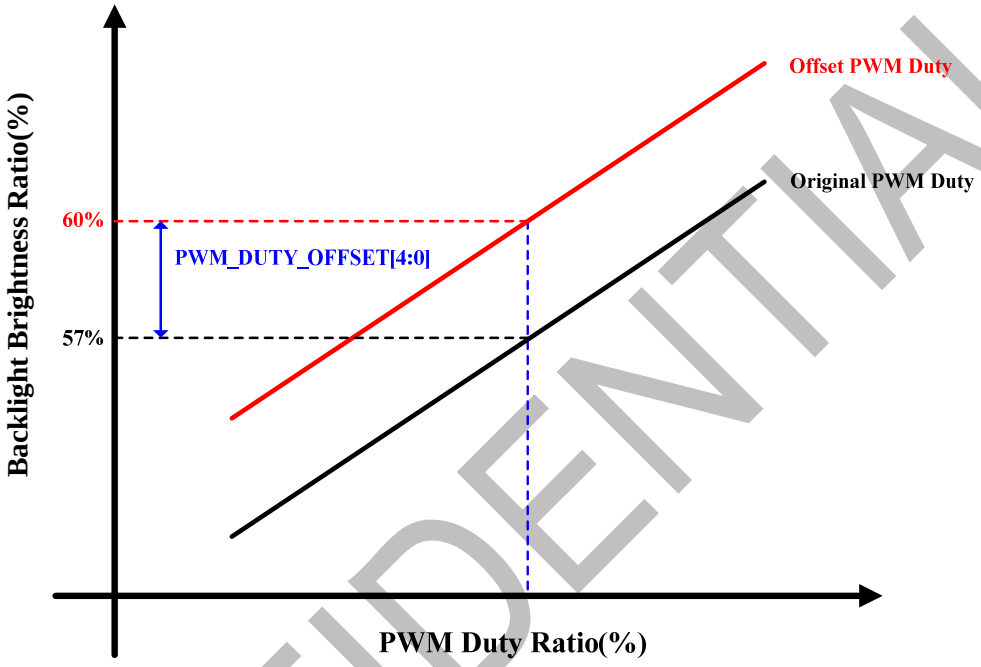
Since the external LED driver needs some stable time to drive the LED backlight, this necessary stable time will reduce the effective PWM duty period. The PWM_DUTY_OFFSET[4:0] is simply used to compensate the loss of PWM duty period. For example, assume original PWM duty of LEDPWM signal is 60%, but the actual backlight brightness driven by LED driver is 57%. User can set "PWM_DUTY_OFFSET[4:0]" to achieve 60% backlight brightness.

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### 7.13.4 Content Adaptive Brightness Control (CABC)

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.There four different modes of CABC can be controlled through register “C[1:0]”(WRCABC).

Descriptions of these four modes are listed below:

1. Off mode: Content Adaptive Brightness Control functionality is totally off.

2. UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible.Target power consumption reduction ratio: 10% or less. User can achieve prefer brightness for UI-Mode by setting the registers “CABC_UI_PWM0[7:0]” ~ “CABC_UI_PWM3[7:0]”.

3. Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%. The RM68120 will automatically estimate a better gamma setting based on image contents. User can achieve prefer brightness for still picture mode by setting the registers “CABC_PWM0[7:0]” ~ “CABC_PWM9[7:0]”.

4. Moving image mode: Optimized for moving image e.g. Video clip. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%. The RM68120 will automatically estimate a better gamma setting based on image contents. User can achieve prefer brightness for still picture mode by setting the registers “CABC_MOV_PWM0[7:0]” ~ “CABC_MOV_PWM9[7:0]”.

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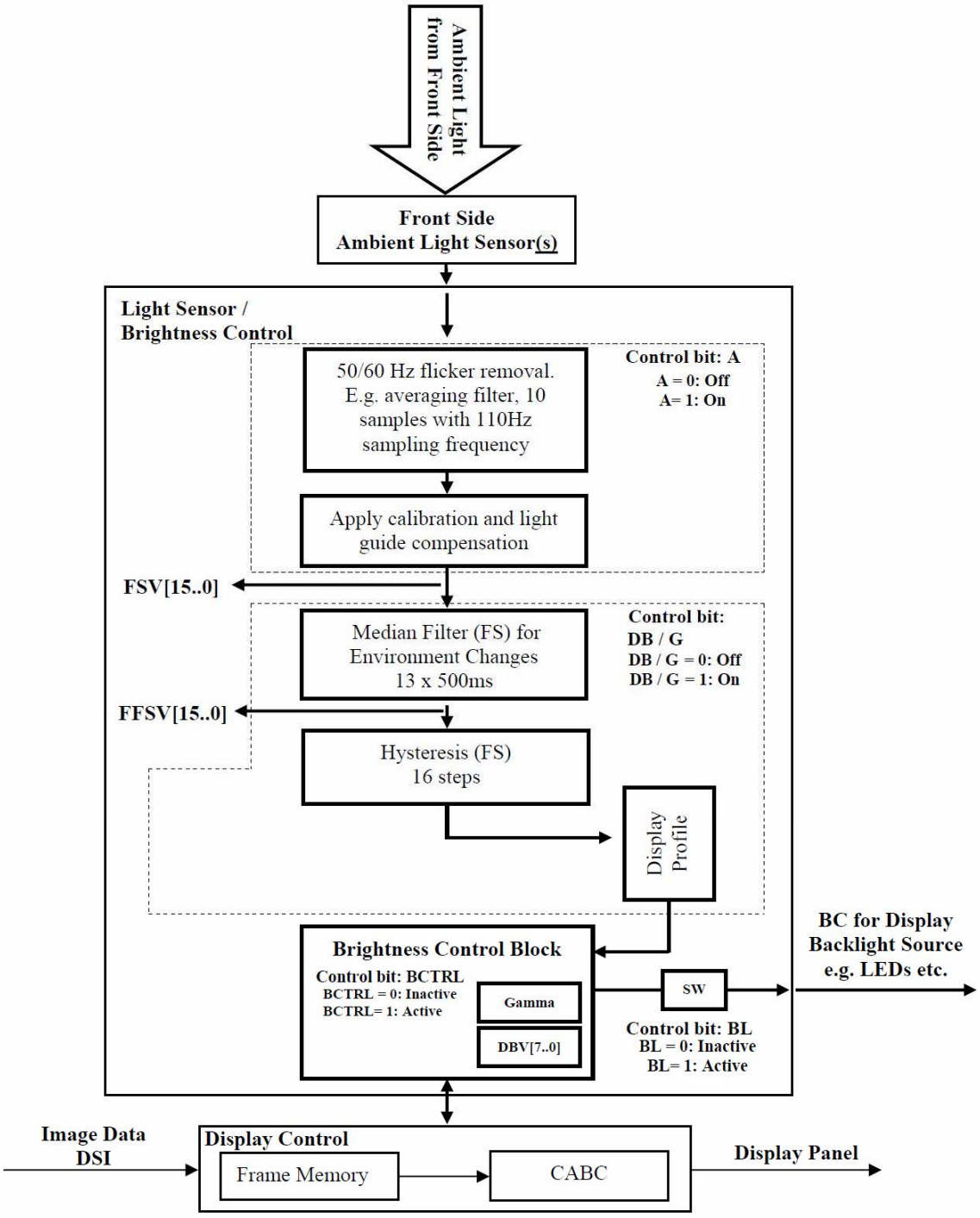
### 7.13.5 Light-Sensor Automatic Brightness Control (LABC)

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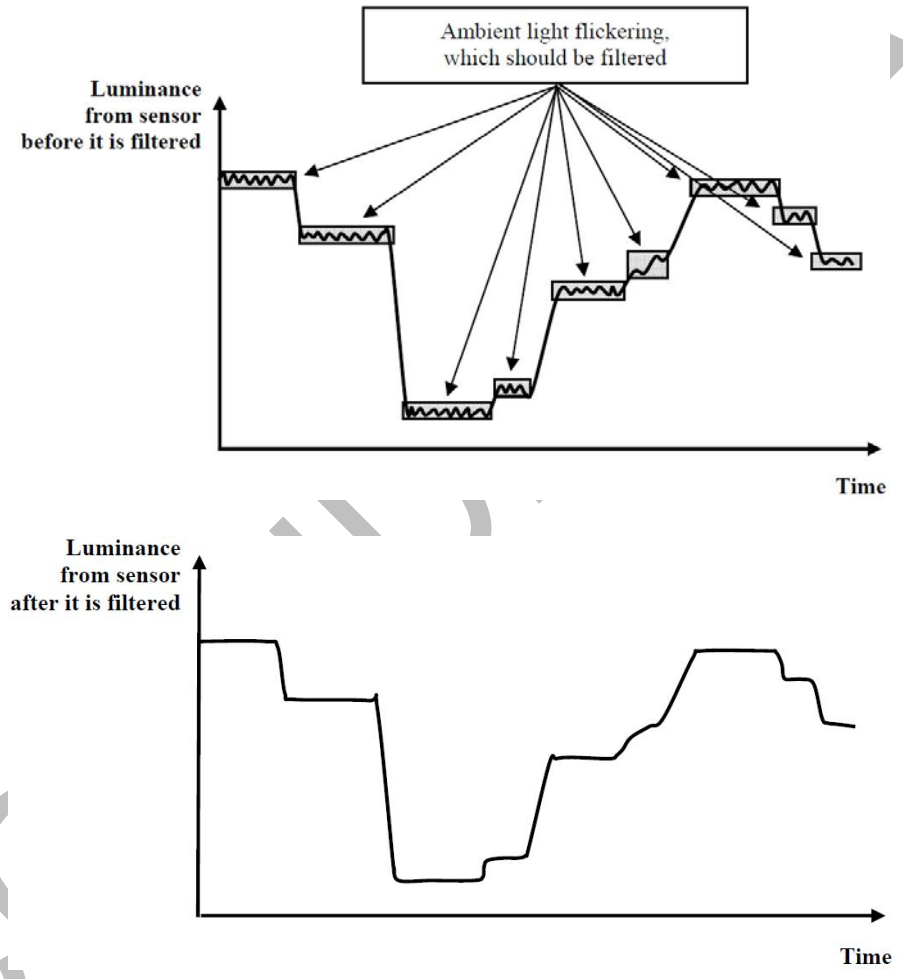
**50/60Hz FLICKER REMOVAL**

"50/60 Hz flicker removal" block is to sample light sensor information via system interface. Same block is for filtering external light source flicker (e.g. 50 and 60 Hz), which maybe present in ambient light source measurements. This functionality is possible to implement with e.g. an averaging filter, 10 samples with 110Hz sampling frequency. These samples are pipelined so that the oldest value is dropped out when a new value is entered (First In-First Out queue). Sampling of ambient light is started after receiving "Write CTRL Display (5300h)" command with applicable parameters.

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**Light Guide Variation Compensation**

Filtered luminance value is inputted into “Apply calibration and light guide compensation” block. “Apply calibration and light guide compensation” block is to calibrate and to compensate variation of light guide which is covered on the ambient light sensor. Compensated luminance value can be read by the user (16 bit value, see chapters: “Read MSBs of FSV Value (5A00h)” and Read LSBs of FSV Value (5B00h)”.

In order to perform a calibration for the ambient light sensor system, “Read Light Sensor Compensation Coefficient Value MSBs (66h)” and “Read Light Sensor Compensation Coefficient Value LSBs (67h)” commands can be used to retrieve measured illuminance. User can define a compensation coefficient for the light guide variation. This additional compensation coefficient CC works as a factor multiplying the ambient light value before the value is returned by “Read FS Value MSBs (5A00h)” and “Read FS Value LSBs (5B00h)” commands or used in hysteresis comparison.

FS_compensated = CC * FS_filtered

FS_compensated: Ambient light information where light guide variation has been taken into account

CC: Compensation coefficient, value range [0.5 – 1.9999]

FS_filtered: Ambient light information after flicker removal

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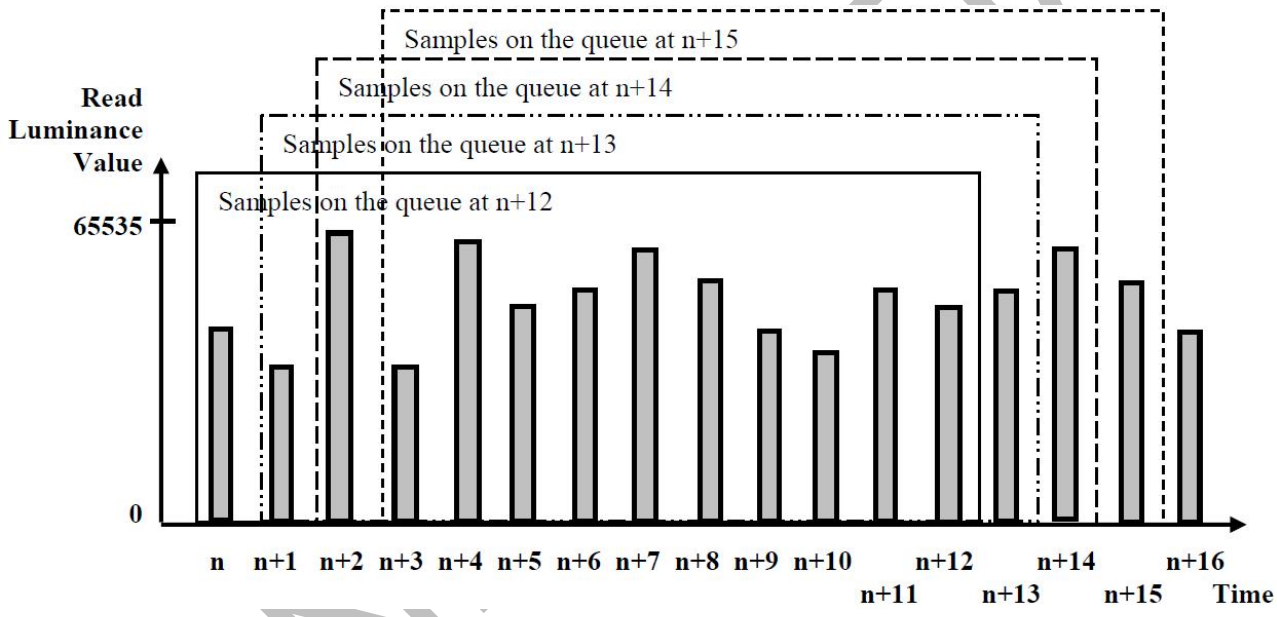
**MEDIAN FILTER**

Median Filter for Environment Changes block is filtering information received from “Apply calibration and light guide compensation” block.

Median filter receives number of values, which are stored in a queue. The length of the queue is 13 samples. The oldest value stored in the queue is also the first value to drop when a new value is queued (First In-First Out queue). The median filter will sort these values of the queue in ascending order. The median filter selects one of those values based on order of magnitude. Selected value is the 7th value which is the median of the sorted queue.

Selected median filter values are inputted into “Hysteresis” block.




Luminance values of this example are defined on the following table.

| Time | Luminance Value (0 – 65535) | Time | Luminance Value (0 – 65535) | Time | Luminance Value (0 – 65535) |
|---|---|---|---|---|---|
| n | 40960 | n+6 | 51200 | n+12 | 47360 |
| n+1 | 30720 | n+7 | 58880 | n+13 | 51200 |
| n+2 | 64000 | n+8 | 53760 | n+14 | 58880 |
| n+3 | 32768 | n+9 | 40960 | n+15 | 53760 |
| n+4 | 62720 | n+10 | 38400 | n+16 | 40960 |
| n+5 | 47360 | n+11 | 51200 | | |

Queues (Read Luminance Values) of this example are defined below.

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| Time | Values of the Queue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10ht | 11th | 12th | 13th |
| n+6 | 40960 | 30720 | 64000 | 32768 | 62720 | 47360 | 51200 | 58880 | 53760 | 40960 | 38400 | 51200 | 47360 |
| n+7 | 30720 | 64000 | 32768 | 62720 | 47360 | 51200 | 58880 | 53760 | 40960 | 38400 | 51200 | 47360 | 51200 |
| n+8 | 64000 | 32768 | 62720 | 47360 | 51200 | 58880 | 53760 | 40960 | 38400 | 51200 | 47360 | 51200 | 58880 |
| n+9 | 32768 | 62720 | 47360 | 51200 | 58880 | 53760 | 40960 | 38400 | 51200 | 47360 | 51200 | 58880 | 53760 |

The median filter will sort these values in ascending order. Example of sorted values are as below table.

| Time | Sorted values in the order of magnitude | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | 11th | 12th | 13th |
| n+6 | 30720 | 32768 | 38400 | 40960 | 40960 | 47360 | 47360 | 51200 | 51200 | 53760 | 58880 | 62720 | 64000 |
| n+7 | 30720 | 32768 | 38400 | 40960 | 47360 | 47360 | 51200 | 51200 | 51200 | 53760 | 58880 | 62720 | 64000 |
| n+8 | 32768 | 38400 | 40960 | 47360 | 47360 | 51200 | 51200 | 51200 | 53760 | 58880 | 58880 | 62720 | 64000 |
| n+9 | 32768 | 38400 | 40960 | 47360 | 47360 | 51200 | 51200 | 51200 | 53760 | 53760 | 58880 | 58880 | 62720 |

The median filter selects one of those values based on order of magnitude. Selected value is the 7th value (values highlighted on the table).

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**HYTERESIS**

"Write Gamma setting (58h)" and "Write Profile Values (50h)".

For each step number 'n', the following values are defined:

An 8-bit value (Vn) which sets the display brightness.

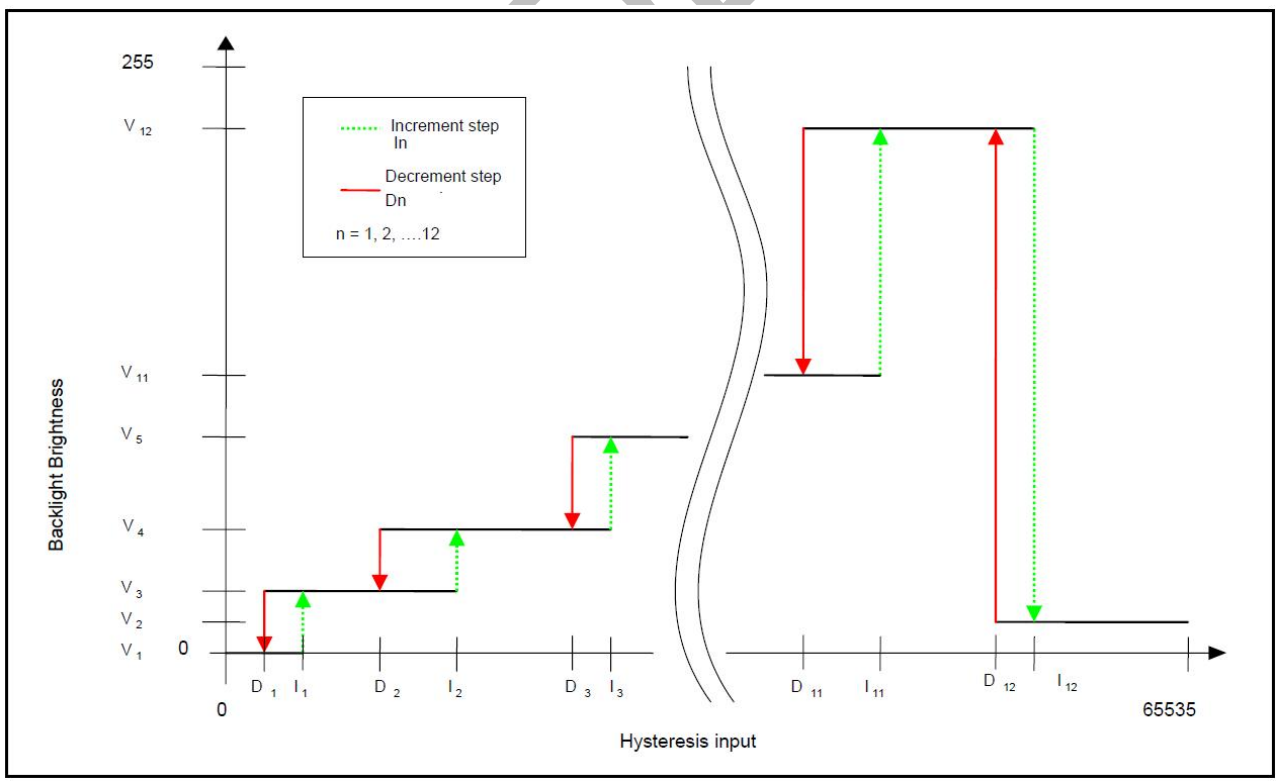
A 16-bit value (In) 'increment step' value. If the output value of the median filter is greater than the previous one, then the In values represent the transition from the step "n" to step "n + 1".

A 16-bit value (Dn) 'decrement step' value. If the output value of the median filter is smaller than the previous one, then the Dn values represent the transition from the step "n" to step "n + 1".

A 4-bit (Gn) 'gamma curve select' value. This uses a 1-hot encoding to select which gamma curve will be used for each step.

Maximum step number (n) is 16.

The following figure shows a graph of hysteresis input value vs. display backlight brightness output for an arbitrary hysteresis curve. For this graph, step 12 is before the last step in the current profile, and so doesn't have any increment or decrement step values associated with it. For the last step both increment and decrement values are set to 65535 (FFFFh).

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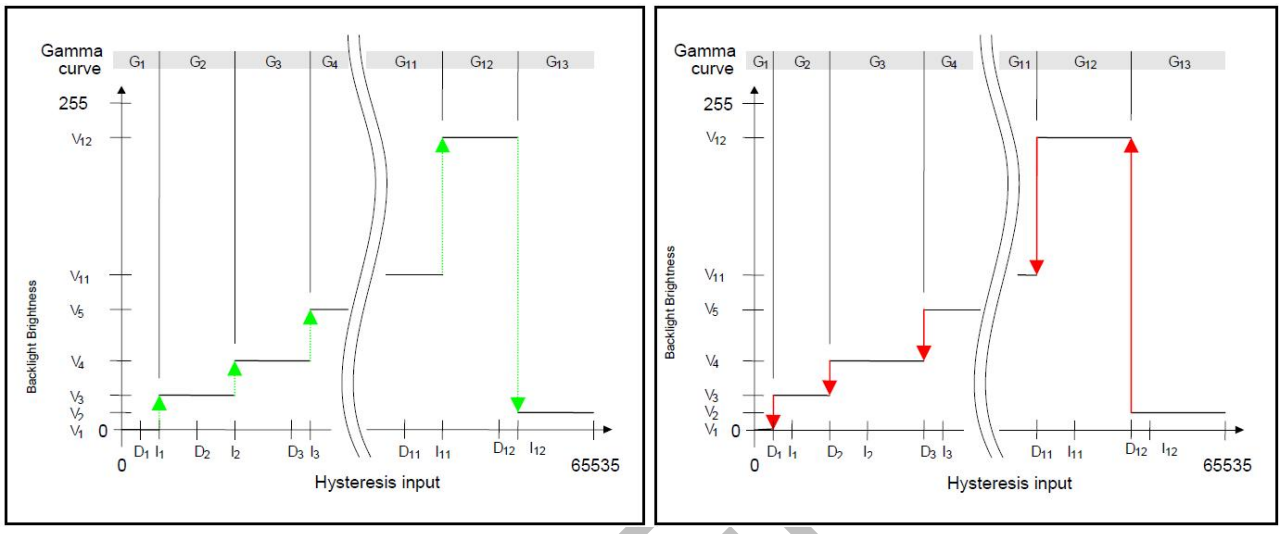
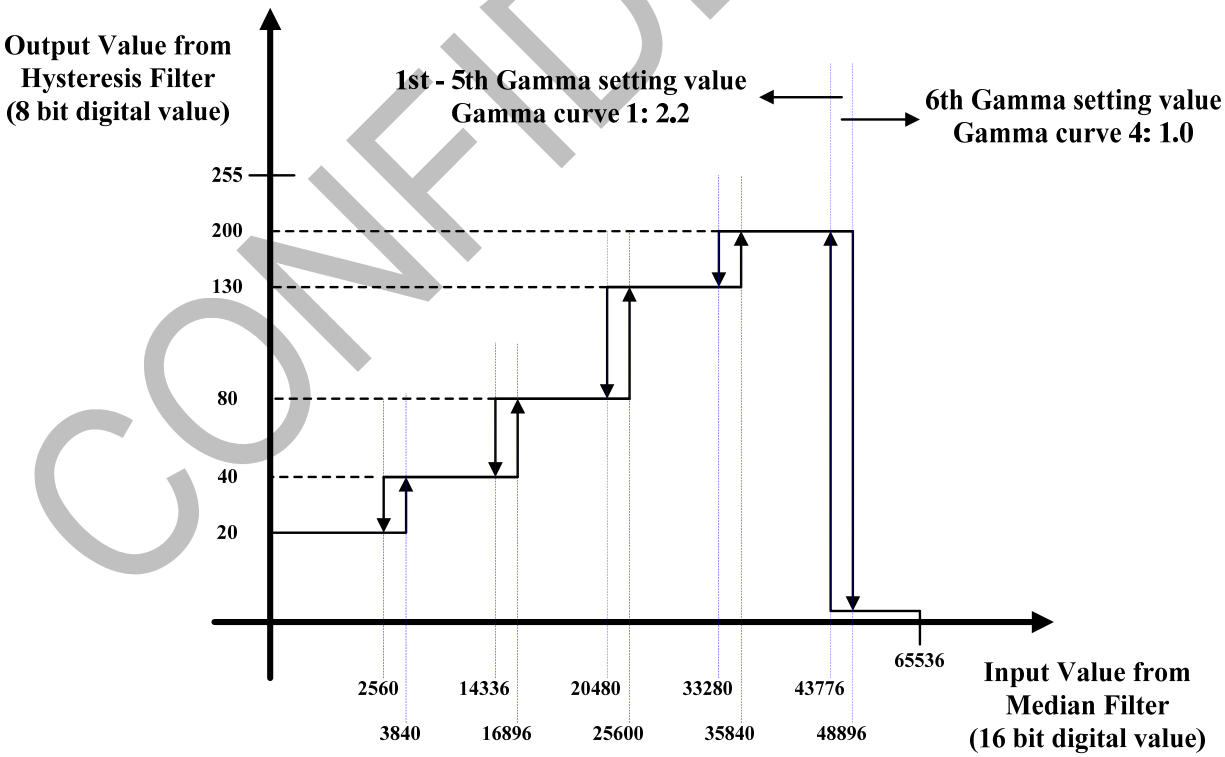
This curve can be split into two separate cases, one for increasing input, and one for decreasing input (see below figure). Once the hysteresis is known to be increasing or decreasing, it can choose correct graph. Then it is relatively simple to go through each of the levels in turn, checking against the increment or decrement values as necessary.




The following example is using 6 steps (6 increment and 6 decrement) for hysteresis 6.

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The following table is specified the relationship between each parameters and step numbers as the above example of hysteresis and profiles.

| Step number (n) | Increment Value (In) | Decrement Value (Dn) | Display Brightness (Vn) | Gamma Curve (Gn) |
|---|---|---|---|---|
| 1 | 3840(F00h) | 2560(A00h) | 20(14h) | 2.2(1h) |
| 2 | 16896(4200h) | 14336(3800h) | 40(28h) | 2.2(1h) |
| 3 | 25600(6400h) | 20480(5000h) | 80(50h) | 2.2(1h) |
| 4 | 35840(8C00h) | 33280(8200h) | 130(82h) | 2.2(1h) |
| 5 | 48896(BF00h) | 43776(AB00h) | 200(C8h) | 2.2(1h) |
| 6 | 65535(FFFFh) | 65535(FFFFh) | 0 | 1.0(8h) |
| 7 | X | X | X | X |
| 8 | X | X | X | X |
| 9 | X | X | X | X |
| 10 | X | X | X | X |
| 11 | X | X | X | X |
| 12 | X | X | X | X |
| 13 | X | X | X | X |
| 14 | X | X | X | X |
| 15 | X | X | X | X |
| 16 | X | X | X | X |

Step number of increment-value and decrement-value is 16 steps. Don't care about the parameter values after "65535 (FFFFh)" of increment value and decrement value, e.g. "X" in the above table. 16th increment and decrement values are always set to "65535 (FFFFh)" internally, if increment and decrement values before 16th parameters are less than "65535 (FFFFh)".

Once the hysteresis curve has been stored using the commands above, the flowchart is used to select the correct hysteresis level after getting median filter output as a reference. Flow chart for adjust correct hysteresis level is as below one.

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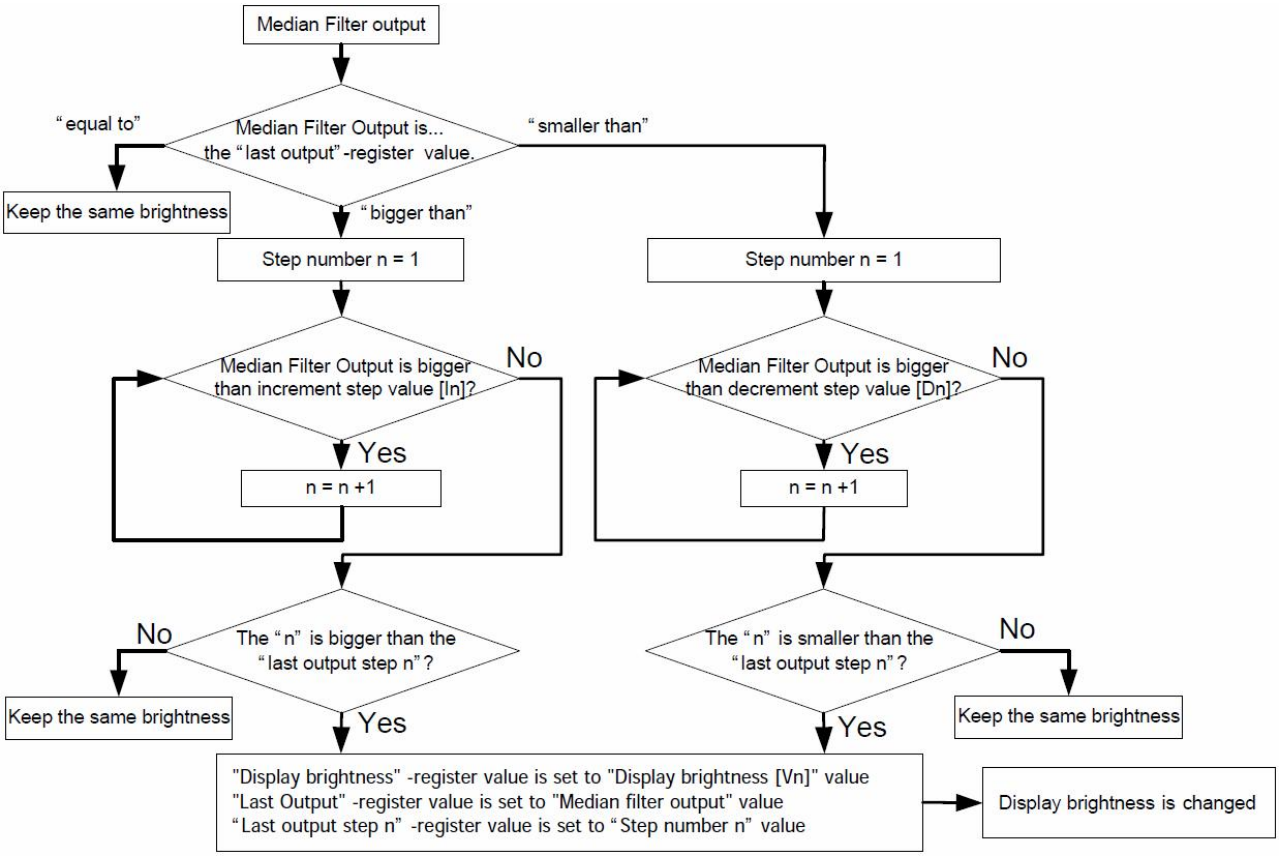


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# 8. Command

## 8.1. Command List

| Operational Code (Hex) | Command | Command(C) /Read(R) /Write(W) | Number Of Parameter |
|---|---|---|---|
| 00h | nop | C | 0 |
| 01h | soft_reset | C | 0 |
| 04h | get_display_ID | R | 3 |
| 05h | get_DSI_err | R | 1 |
| 0Ah | get_power_mode | R | 1 |
| 0Bh | get_address_mode | R | 1 |
| 0Ch | get_pixel_format | R | 1 |
| 0Dh | get_display_mode | R | 1 |
| 0Eh | get_signal_mode | R | 1 |
| 0Fh | get_diagnostic_result | R | 1 |
| 10h | enter_sleep_mode | C | 0 |
| 11h | exit_sleep_mode | C | 0 |
| 12h | enter_partial_mode | C | 0 |
| 13h | enter_normal_mode | C | 0 |
| 20h | exit_invert_mode | C | 0 |
| 21h | enter_invert_mode | C | 0 |
| 22h | set_all_pixel_off | C | 0 |
| 23h | set_all_pixel_on | C | 0 |
| 26h | Gamma_curve_setlect | W | 1 |
| 28h | set_display_off | C | 0 |
| 29h | set_display_on | C | 0 |
| 2Ah | set_column_address | W | 4 |
| 2Bh | set_page_address | W | 4 |
| 2Ch | write_memory_start | W | Variable |
| 2Eh | read_memory_start | R | Variable |
| 30h | set_partial_area | W | 4 |
| 33h | set_scroll_area | W | 6 |
| 34h | set_tear_off | C | 0 |
| 35h | set_tear_on | W | 1 |
| 36h | set_address_mode | W | 1 |
| 38h | exit_idle_mode | C | 0 |
| 39h | enter_idle_mode | C | 0 |
| 3Ah | set_pixel_format | W | 1 |
| 3Ch | write_memory _continue | W | Variable |
| 3Eh | read_memory _continue | R | Variable |
| 44h | set_tear_scanline | W | 2 |
| 45h | get_scanline | R | 2 |
| 4Fh | set_deep_standby_mode | W | 1 |

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| Operational Code (Hex) | Command | Command(C) /Read(R) /Write(W) | Number Of Parameter |
|---|---|---|---|
| 50h | set_profile_value_for_display | W | 16 |
| 51h | set_display_brightness | W | 1 |
| 52h | get_display_brightness | R | 1 |
| 53h | set_control_display | W | 1 |
| 54h | get_control_display | R | 1 |
| 55h | set_cabc_mode | W | 1 |
| 56h | get_cabc_mode | R | 1 |
| 57h | set_hysteresis | W | 32 |
| 58h | set_gamma_setting | W | 8 |
| 5Ah | get_FS_value_MSBs | R | 1 |
| 5Bh | get_FS_value_LSBs | R | 1 |
| 5Ch | get_median_filter_FS_value_MSBs | R | 1 |
| 5Dh | get_median_filter_FS_value_LSBs | R | 1 |
| 5Eh | set_cabc_min_brightness | W | 1 |
| 5Fh | get_cabc_min_brightness | R | 1 |
| 65h | set_light_sensor_compensation_coefficient | W | 2 |
| 66h | get_LSCC_MSBs | R | 1 |
| 67h | get_LSCC_LSBs | R | 1 |
| 70h | get_black/white low bit | R | 1 |
| 71h | get_Bkx | R | 1 |
| 72h | get_Bky | R | 1 |
| 73h | get_Wx | R | 1 |
| 74h | get_Wy | R | 1 |
| 75h | get_red/green low bit | R | 1 |
| 76h | get_Rx | R | 1 |
| 77h | get_Ry | R | 1 |
| 78h | get_Gx | R | 1 |
| 79h | get_Gy | R | 1 |
| 7Ah | get_blue/Acolor low bit | R | 1 |
| 7Bh | get_Bx | R | 1 |
| 7Ch | get_By | R | 1 |
| 7Dh | get_Ax | R | 1 |
| 7Eh | get_Ay | R | 1 |
| A1h | read_DDB_start | R | 5 |
| A8h | read_DDB_continue | R | 5 |
| AAh | read_first_checksum | R | 1 |
| AFh | read_continue_checksum | R | 1 |
| DAh | read_ID1 | R | 1 |
| DBh | read_ID2 | R | 1 |
| DCh | read_ID3 | R | 1 |

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## 8.2. Command Description

### NOP (0000h)

| 0000H | NOP (No Operation) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D17-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.<br>X = Don't care. | | | | | | | | | | | | |
| Restriction | None | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | N/A |
| SW Reset | N/A |
| HW Reset | N/A |

| Flow Chart | None |
|---|---|

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**SWRESET(0100h) : Software Reset**

| 0100H | SWRESET(Software Reset) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)<br>Note: The Frame Memory contents are affected by this command.<br>X = Don't care | | | | | | | | | | | | |
| Restriction | Software Reset Command cannot be sent during Sleep Out sequence.<br>Any new command is cannot be sent for 10-frame period until the RM68120 enters Sleep-In mode. Do not send any command. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | N/A |
| SW Reset | N/A |
| HW Reset | N/A |

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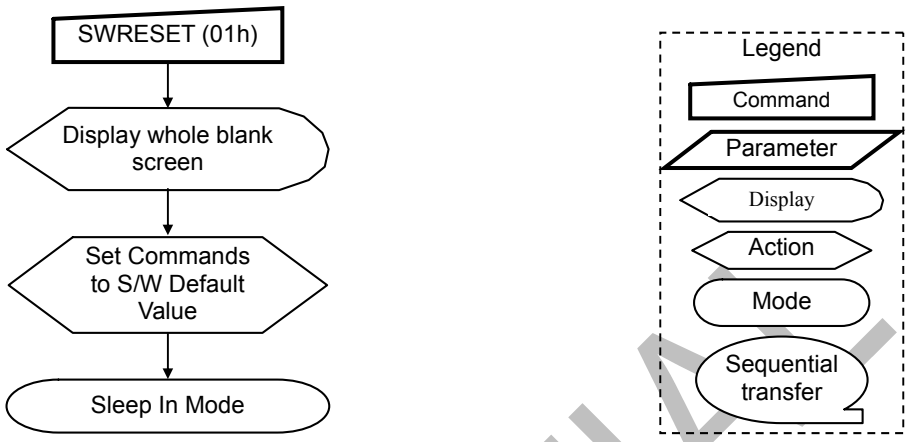
| | |
|---|---|
| Flow Chart |  |



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**RDDID(0400h~0402h) : Read Display ID**

| 0400H | RDDID | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 00h | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 1st | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd | 1 | ↑ | 1 | 00h | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | 00 |
| 3rd | 1 | ↑ | 1 | 00h | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | 80 |
| 4th | 1 | ↑ | 1 | 00h | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | 00 |
| Parameter | - | | | | | | | | | | | | |
| Description | The 1st parameter (ID1): the module's manufacture ID<br>The 2nd parameter (ID2): the module/driver version ID<br>The 3rd parameter (ID3): the module/driver ID<br>Note: Commands RDID1/2/3 (DAh/DBh/DCh) read data correspond to the parameter 1, 2, 3 of command 04h, respectively. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP value | ID1=00h / ID2=80h / ID3=00h |
| SW Reset | MTP value | ID1=00h / ID2=80h / ID3=00h |
| HW Reset | MTP value | ID1=00h / ID2=80h / ID3=00h |

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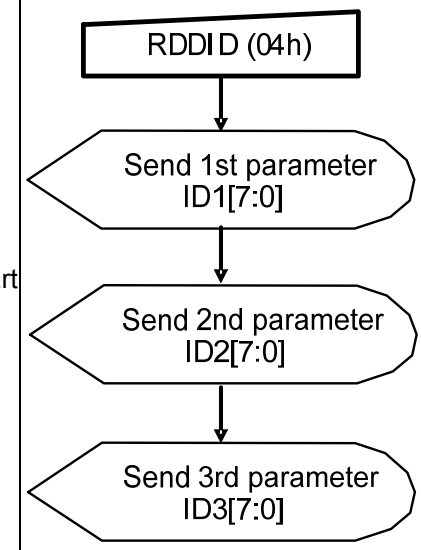
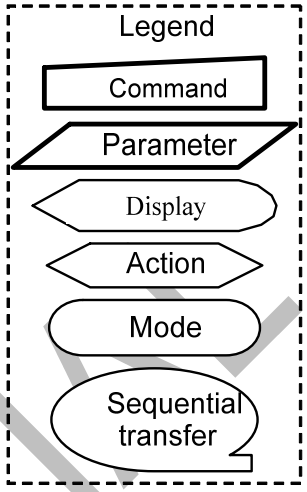
Flow Chart

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**RDNUMED(0500h) : Read Number of Errors on DSI**

| 0500H | RDNUMED | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| 1st | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd | 1 | ↑ | 1 | x | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | 00 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.<br>P[6..0] bits are telling a number of the parity errors.<br>P[7] is set to “1” if there is overflow with P[6..0] bits.<br>P[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed).<br>This command is used for MIPI DSI only. It is no function for others interface operation. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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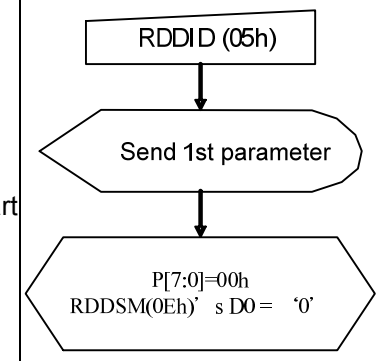
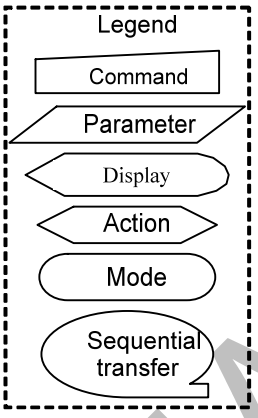
Flow Chart

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**RDDPM (0A00h) : Read Display Power Mode**

| 0A00H | RDDPM (Read Display Power Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 08 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | BSTON | Booster Voltage Status | '1'=Booster on,<br>'0'=Booster off |
| D6 | IDMON | Idle Mode On/Off | '1' = Idle Mode On,<br>'0' = Idle Mode Off |
| D5 | PTLON | Partial Mode On/Off | '1' = Partial Mode On,<br>'0' = Partial Mode Off |
| D4 | SLPON | Sleep In/Out | '1' = Sleep Out,<br>'0' = Sleep In |
| D3 | NORON | Display Normal Mode On/Off | '1' = Normal Display,<br>'0' = Partial Display |
| D2 | DISON | Display On/Off | '1' = Display On,<br>'0' = Display Off |
| D1 | Reserved | | 0 |
| D0 | Reserved | | 0 |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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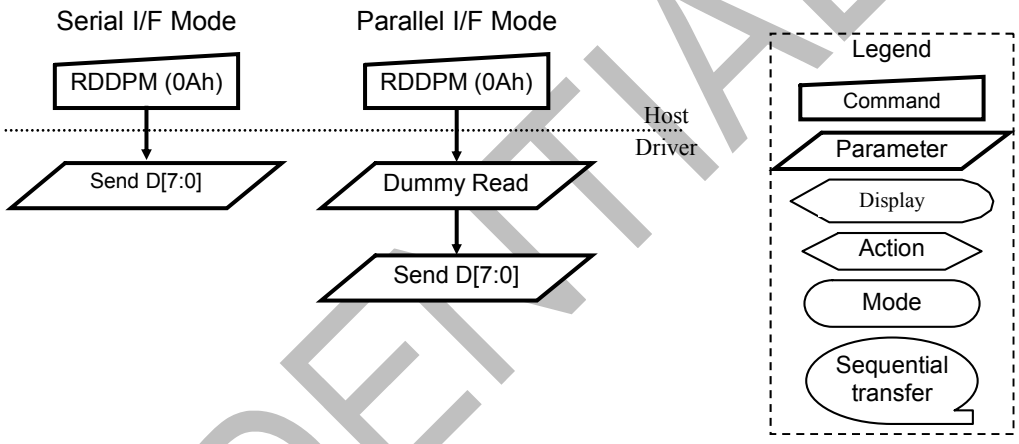
Default

| Status | Default Value |
|---|---|
| Power On Sequence | 08h |
| SW Reset | 08h |
| HW Reset | 08h |

Flow Chart

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**RDDMADCTR (0B00h): Read Display MADCTR**

| 0B00H | RDDMADCTR (Read Display MADCTR) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | MY | Row Address Order | '1' = Bottom to Top (36H-D7='1')<br>'0' = Top to Bottom (36H- D7='0') |
| D6 | MX | Column Address Order | '1' = Right to Left (MADCTL D6='1')<br>'0' = Left to Right (MADCTL D6='0') |
| D5 | MV | Row/Column Order (MV) | '1' = Row/column exchange(36H-D5='1')<br>'0' = Normal (36H-D5='1') |
| D4 | ML | Vertical Refresh Order | '1' =LCD Refresh Top to Bottom<br>'0' =LCD Refresh Bottom to Top |
| D3 | RGB | RGB/BGR Order | '1' =BGR, "0"=RGB |
| D2 | MH | Horizontal Refresh Order | '0' = LCD Refresh Left to Right<br>'1' = LCD Refresh Right to Left |
| D1 | RSMX | Horizontal Flip | '0' = Normal display(36H-D1='1')<br>'1' = Flipped display(36H-D1='1') |
| D0 | RSMY | Vertical Flip | '0' = Normal display(36H-D0='1')<br>'1' = Flipped display(36H-D0='1') |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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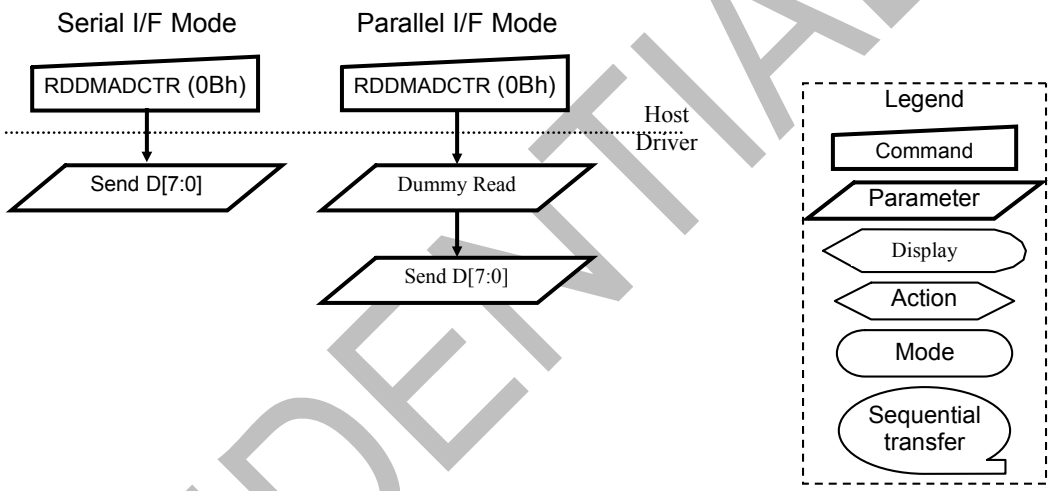
Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | No Change |
| HW Reset | 00h |

Flow Chart

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**RDDCOLMOD (0C00h): Read Display Pixel Format**

| 0C00H | RDDCOLMOD (Read Display Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 66 |

Description

This command indicates the current status of the display as described in the table below:

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | Reserved | | '0' |
| D6 | VIPF[2] | DPI Pixel Format(RGB Interface Color Format) | '101' = 16-bits / pixel,<br>'110' = 18-bits / pixel,<br>'111' = 24-bits / pixel,<br>others are no define |
| D5 | VIPF[1] | | |
| D4 | VIPF[0] | | |
| D3 | Reserved | | '0' |
| D2 | IFPF[2] | DBI Pixel Format(Control Interface Color Format) | '101' = 16-bits / pixel,<br>'110' = 18-bits / pixel,<br>'111' = 24-bits / pixel,<br>others are no define |
| D1 | IFPF[1] | | |
| D0 | IFPF[0] | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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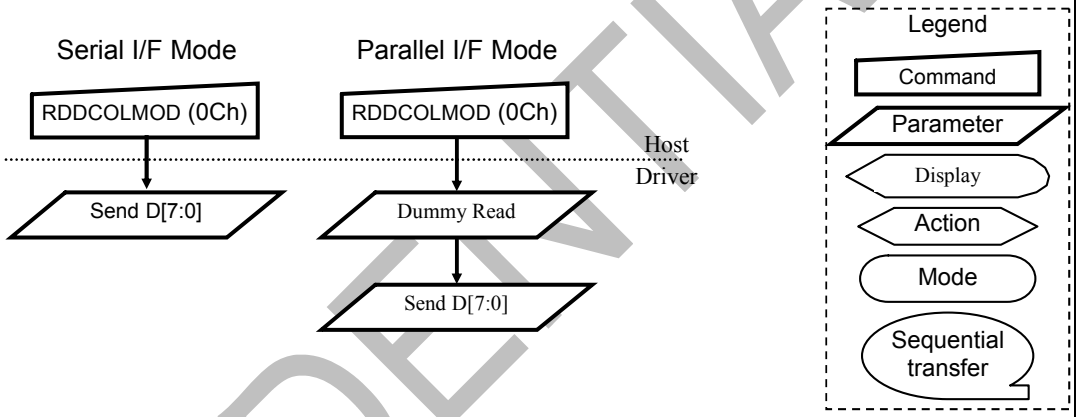
Default

| Status | Default Value |
|---|---|
| Power On Sequence | 66h |
| SW Reset | No Change |
| HW Reset | 66h |

Flow Chart

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**RDDIM (0D00h): Read Display Image Mode**

| 0D00H | RDDIM (Read Display Image Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| 1st Parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd Parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

**Description**

The display module returns the display image mode status.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | Reserved | | '0' |
| D6 | Reserved | | '0' |
| D5 | INVON | Inversion On/Off | "1" = Inversion is On,<br>"0" = Inversion is Off |
| D4 | ALLON | All Pixel On | '0' = Normal display<br>'1' = White display |
| D3 | ALLOFF | All Pixel Off | '0' = Normal display<br>'1' = Black display |
| D2~D0 | GAMSET | Gamma Curve Selection | '000' = GC0, '001' = GC1<br>'010' = GC2, '011' = GC3 |

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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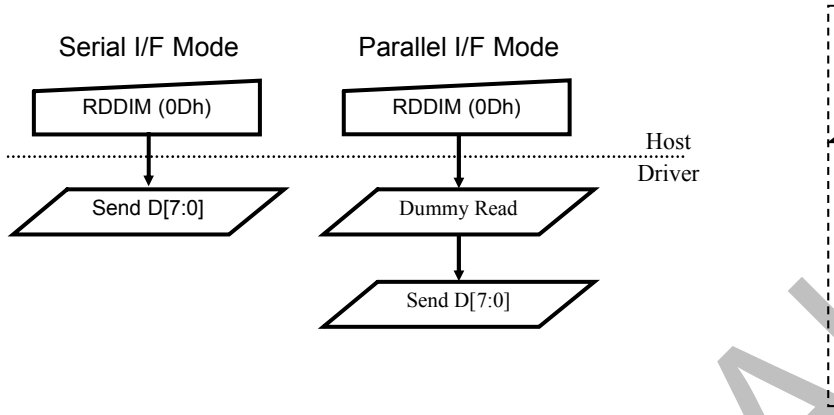
Flow Chart

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**RDDSM (0E00h): Read Display Signal Mode**

| 0E00H | RDDSM (Read Display Signal Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

Description

The display module returns the Display Signal Mode.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | TEON | Tearing Effect Line On/Off | "1" = On, "0" = Off |
| D6 | TELOM | Tearing effect line mode | "0" = mode1,<br>"1" = mode2 |
| D5 | HS | Horizontal Sync On/Off | '0' = HS bit is 0<br>'1' = HS bit is 1 |
| D4 | VS | Vertical Sync On/Off | '0' = VS bit is 0<br>'1' = VS bit is 1 |
| D3 | PCLK | Pixel Clock On/Off | '0' = PCLK is Off<br>'1' = PCLK is On |
| D2 | DE | Data Enable On/Off | '0' = DE is 0<br>'1' = DE is 1 |
| D1 | Reserved | | '0' |
| D0 | Error on DSI | Error on DSI | '0' = No Error<br>'1' = Error |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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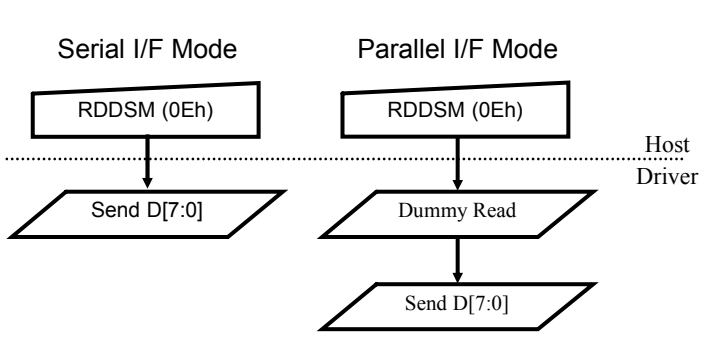
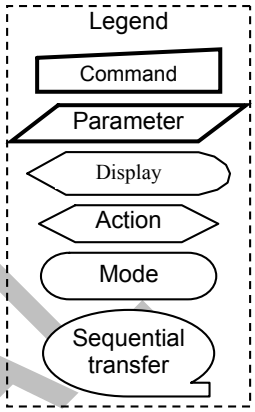
Flow Chart

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**RDDSDR (0F00h): Read Display Self-Diagnostic Result**

| 0F00H | RDDSDR (Read Display Self-Diagnostic Result) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 1st Parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd Parameter | 1 | ↑ | 1 | x | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00 |

**Description**

The display module returns the self-diagnostic results following a Sleep Out command.

| Bit | Symbol | Description | Comment |
|---|---|---|---|
| D7 | RELD | Register Loading Detection | |
| D6 | FUND | Functionality Detection | |
| D5 | CAD | Chip Attachment Detection | |
| D4 | DGBD | Display Glass Break Detection | |
| D3 | Reserved | | '0' |
| D2 | Reserved | | '0' |
| D1 | Reserved | | '0' |
| D0 | CSC | Checksums Comparsion | '0' = Same<br>'1' = Not Same |

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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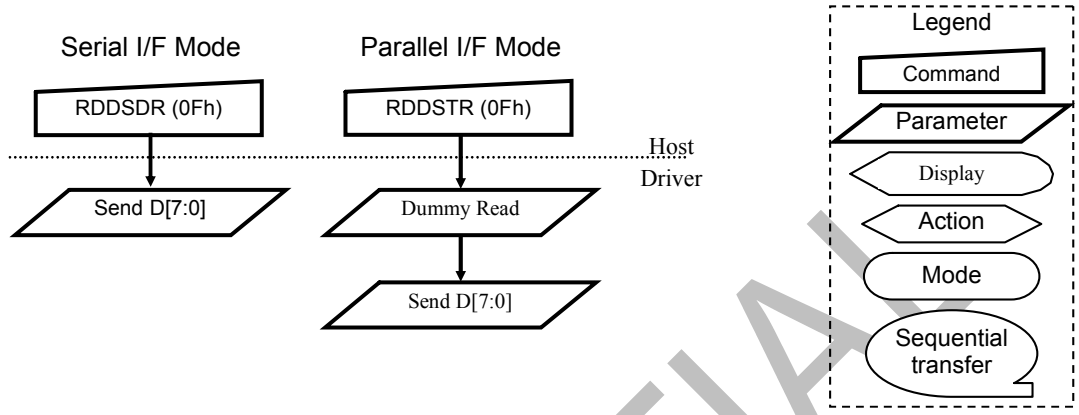
Flow Chart

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**SLPIN (1000h): Sleep In**

| 1000H | SLPIN (Sleep In) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to enter the Sleep mode.<br>This command causes the AMOLED module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal mode. | | | | | | | | | | | | |
| Restriction | This command has no effect when the display module is already in Sleep mode.<br>The host processor must wait 5 milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending a Sleep Out command before sending an Sleep In command. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |
| Default | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep In Mode |
| SW Reset | Sleep In Mode |
| HW Reset | Sleep In Mode |

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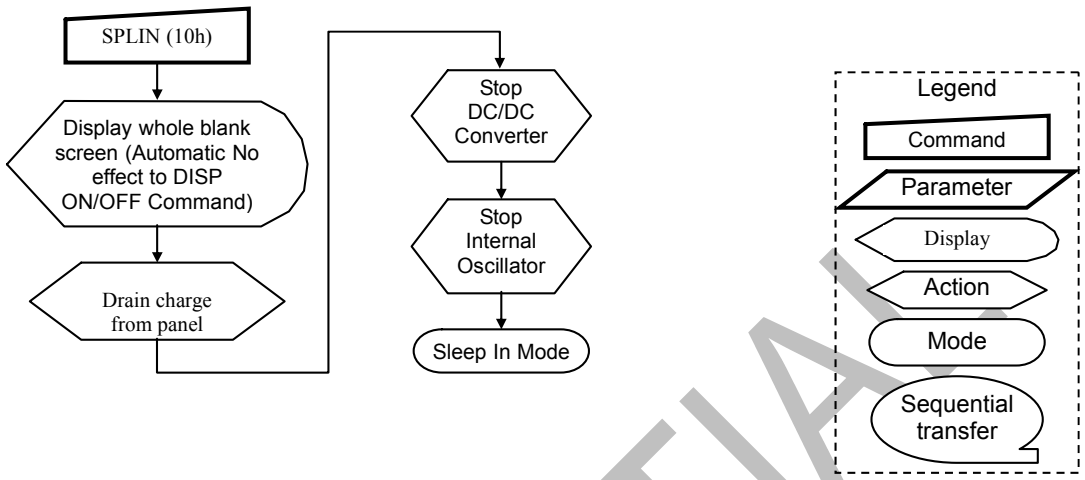
Flow Chart

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**SLPOUT (1100h): Sleep Out**

| 1100H | SLPOUT (Sleep Out) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode. | | | | | | | | | | | | |
| Restriction | This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.<br>The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |
| Default | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep In Mode |
| SW Reset | Sleep In Mode |
| HW Reset | Sleep In Mode |

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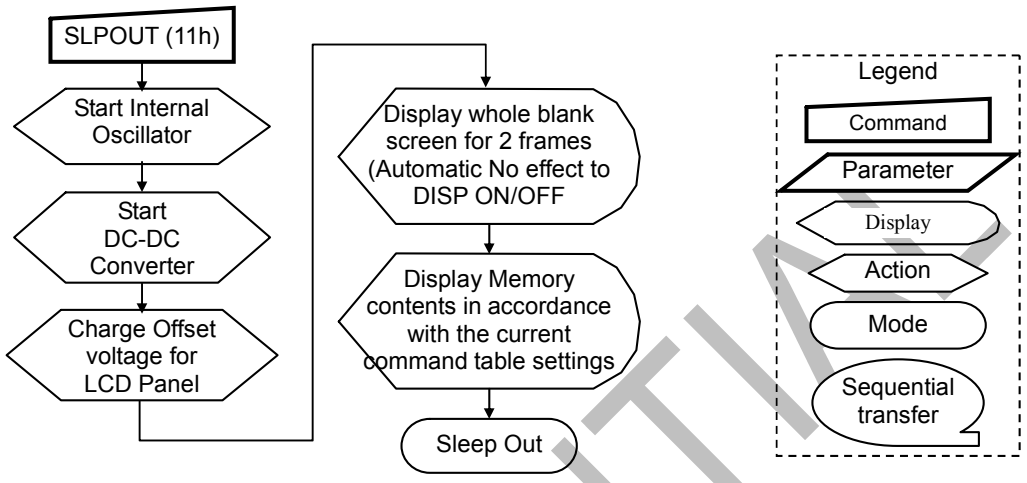
Flow chart

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**PTLON (1200h): Partial Display Mode On**

| 1200H | PTLON (Partial Display Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command.<br>To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode. | | | | | | | | | | | | |
| Restriction | This command has no effect when Partial Display Mode is already active. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Normal display mode On |
| SW Reset | Normal display mode On |
| HW Reset | Normal display mode On |

Flow Chart

Refer to Partial Area (30h)

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**NORON (1300h): Normal Display Mode On**

<table>
<tr><th>1300H</th><th colspan="13">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off.<br>The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is already active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">Refer to the description of Partial Area (3000h)</td></tr>
</table>

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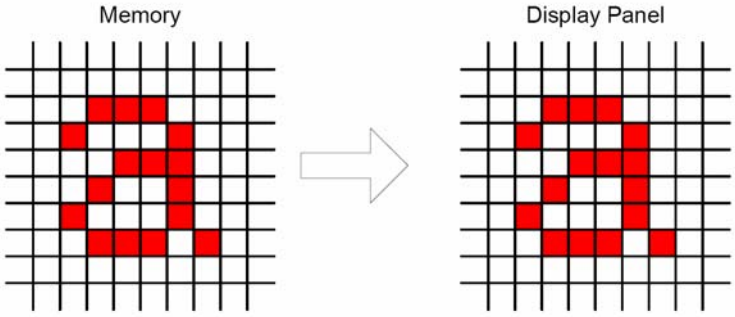
**INVOFF (2000H): Display Inversion Off**

| 2000H | INVOFF (Display Inversion Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.   | | | | | | | | | | | | |
| Restriction | This command has no effect when the display module is not inverting the display image. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| SW Reset | Display Inversion off |
| HW Reset | Display Inversion off |

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| | |
|---|---|
| Flow Chart | |



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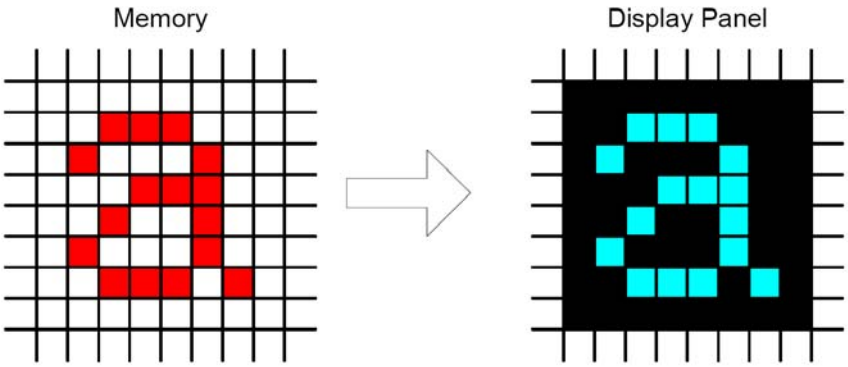
**INVON (2100H): Display Inversion On**

| 2100H | INVON (Display Inversion On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in inversion on mode. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| SW Reset | Display Inversion off |
| HW Reset | Display Inversion off |

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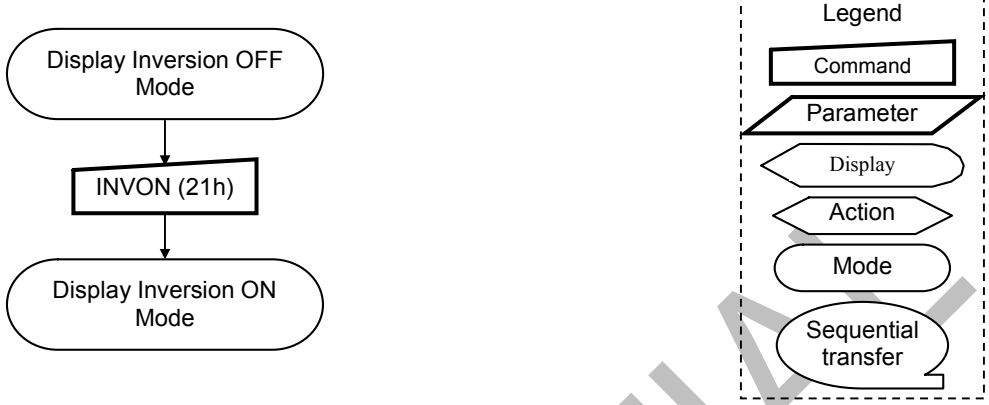
| | |
|---|---|
| Flow Chart |  |



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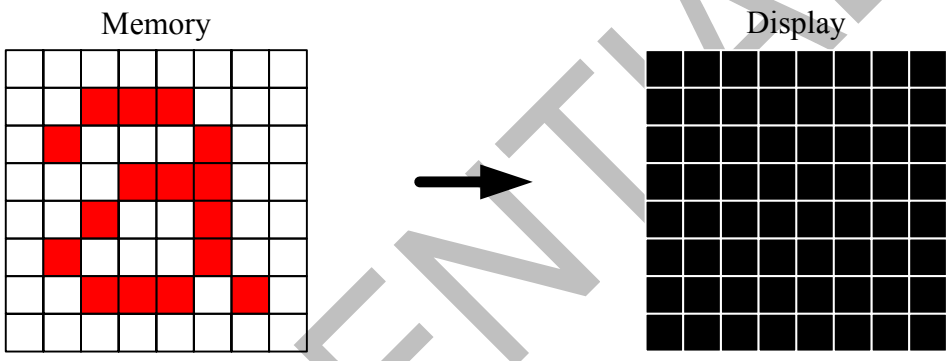
**ALLPOFF (2200H): All Pixel Off**

| 2200H | ALLPOFF | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>  <br>"All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| SW Reset | Display Inversion off |
| HW Reset | Display Inversion off |

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| | |
|---|---|
| Flow Chart | |



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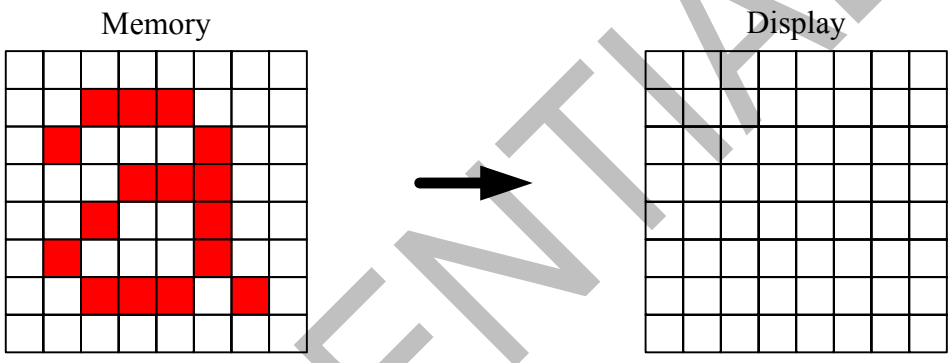
**ALLPON (2300H): All Pixel On**

| 2300H | ALLPON | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.<br>This command makes no change of contents of frame memory.<br>This command does not change any other status.<br>  <br>"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| SW Reset | Display Inversion off |
| HW Reset | Display Inversion off |

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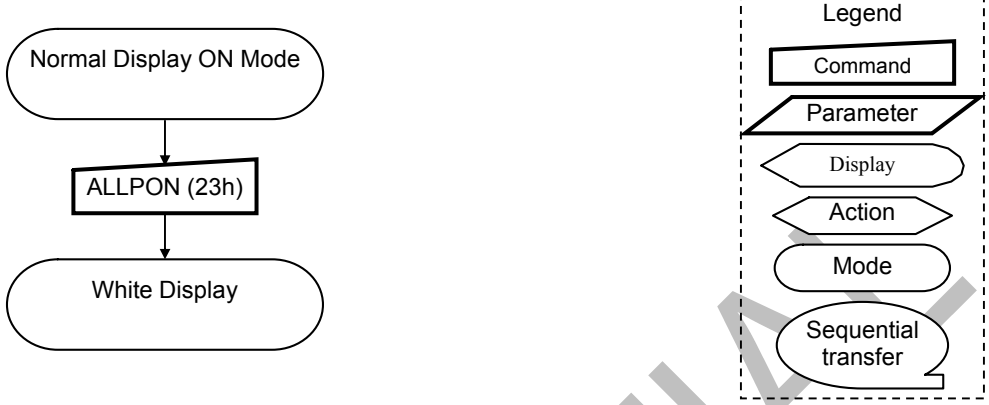
| | |
|---|---|
| Flow Chart |  |



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**GAMSET (2600H): Gamma Set**

<table>
<tr><th>2600H</th><th colspan="13">GAMSET</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>GC7</td><td>GC6</td><td>GC5</td><td>GC4</td><td>GC3</td><td>GC2</td><td>GC1</td><td>GC0</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.
<table>
<tr><th>GC[7:0]</th><th>Parameter</th><th>Curve</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve (G2.2)</td></tr>
<tr><td>02h</td><td>GC1</td><td>Reserved</td></tr>
<tr><td>04h</td><td>GC2</td><td>Reserved</td></tr>
<tr><td>08h</td><td>GC3</td><td>Reserved</td></tr>
</table>
Note: All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>SW Reset</td><td>01h</td></tr>
<tr><td>HW Reset</td><td>01h</td></tr>
</table>
</td></tr>
</table>

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| | |
|---|---|
| Flow Chart | |



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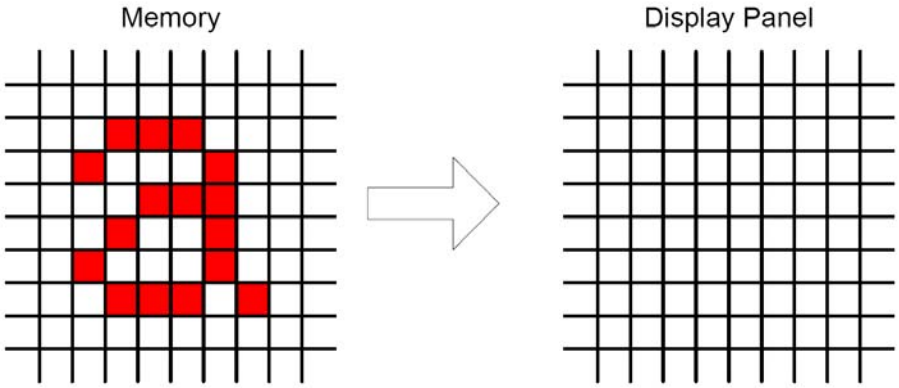
**DISPOFF (2800h): Display Off**

| 2800H | DISPOFF (Display Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display off mode. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Off |
| SW Reset | Display Off |
| HW Reset | Display Off |

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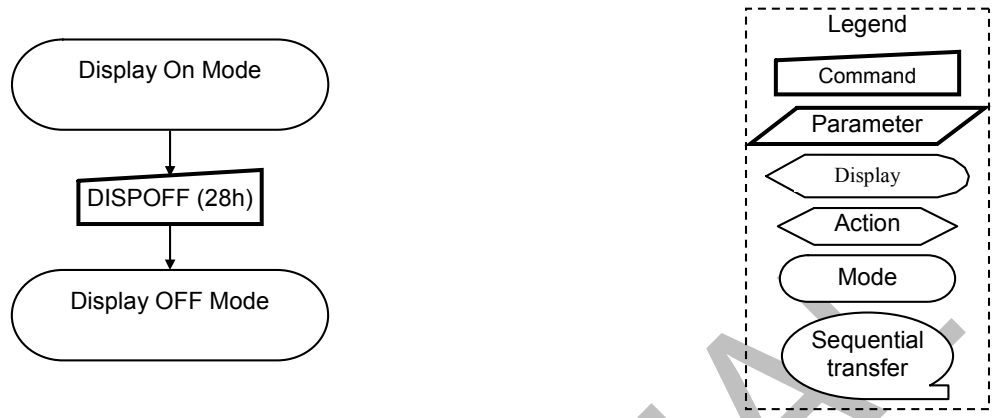
| | |
|---|---|
| Flow Chart |  |



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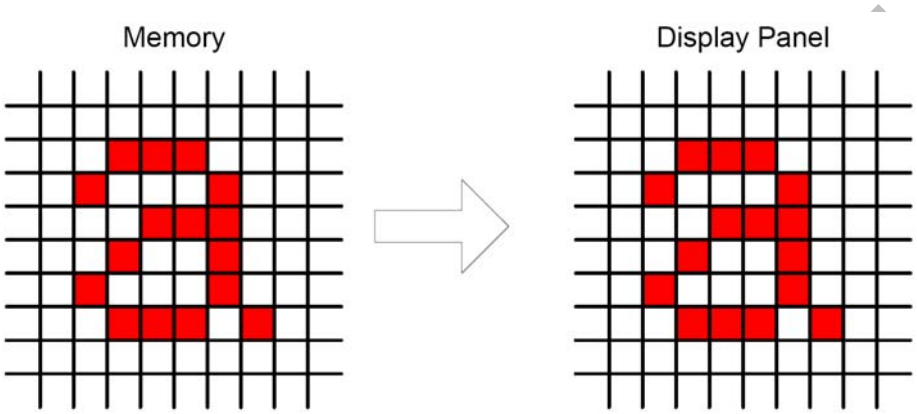
**DISPON (2900h): Display On**

| 2900H | DISPON (Display On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 |
| Parameter | No Parameter | | | | | | | | | | | | |
| Description | This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.<br>  | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in display on mode. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display Off |
| SW Reset | Display Off |
| HW Reset | Display Off |

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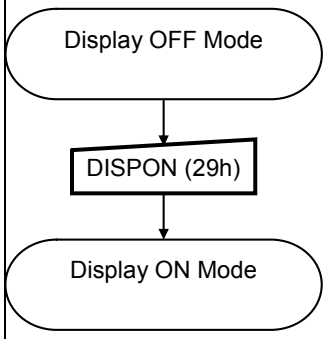
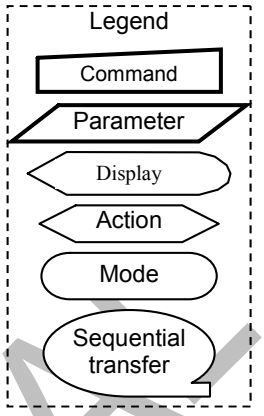
Flow Chart

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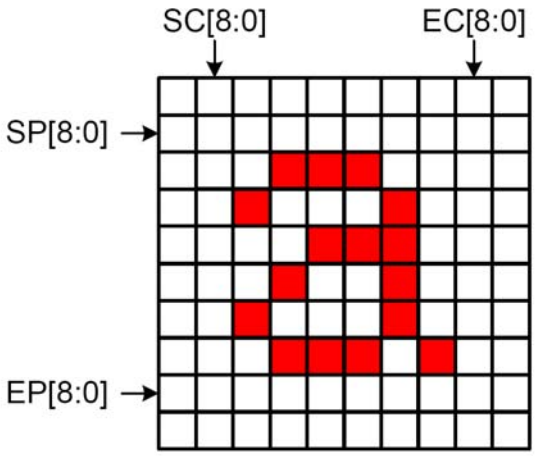
**CASET (2A00h): Column Address Set**

| 2A00H | CASET (Column Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC8 | 00 |
| 2nd parameter | 1 | 1 | ↑ | x | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | 00 |
| 3rd parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EC8 | 01 |
| 4th parameter | 1 | 1 | ↑ | x | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 | DF |
| Description | This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.   | | | | | | | | | | | | |

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**Restriction**

SC [8:0] always must be equal to or less than EC[8:0]

7 GCM[7:0] = 70h : 480x864
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 863(035Fh)

8 GCM[7:0] = 6Bh : 480x854
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 853(0355h)

9 GCM[7:0] = 50h : 480x800
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 799(031Fh)

10 GCM[7:0] = 28h : 480x720
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 719(02CFh)

11 GCM[7:0] = 00h : 480x640
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 639(027Fh)

12 GCM[7:0] = FEh : 480x360
MV(36h-B5)=0 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 479(01DFh)
MV(36h-B5)=1 : Parameter range : 0 ≦ SC[8:0] ≦ EC[8:0] ≦ 359(0167h)

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | SC[8:0] | EC[8:0](36h-B5=0) |
| Power On Sequence | 0000h | 01DFh |
| SW Reset | 0000h | 01DFh |
| HW Reset | 0000h | 01DFh |

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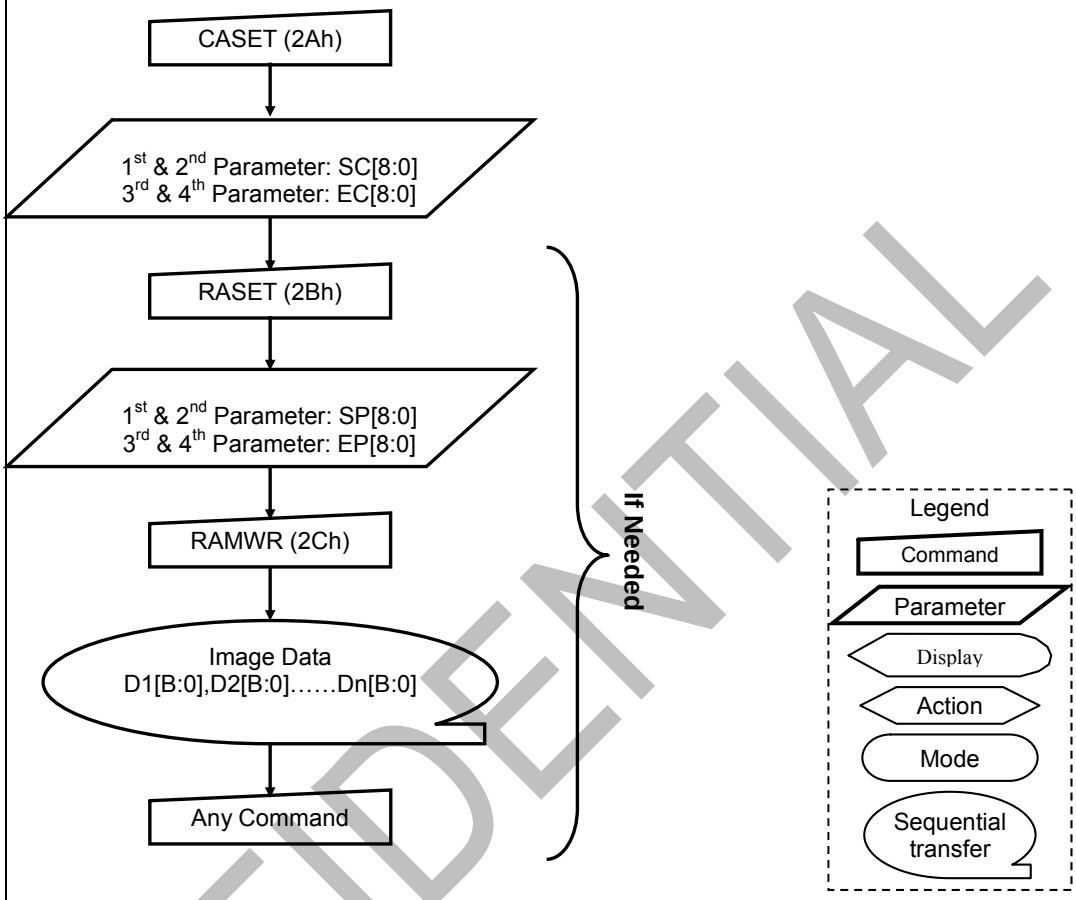
Flow chart




Note : B=23

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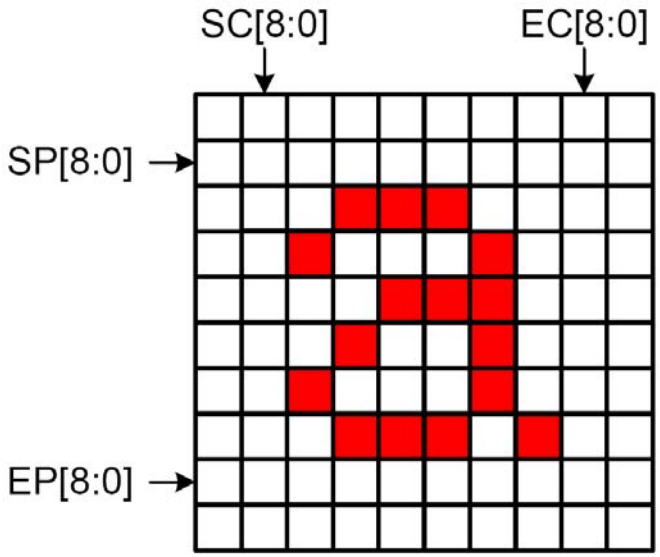
**RASET (2B00h): Row Address Set**

| 2B00H | RASET (Row Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SP8 | 00 |
| 2nd parameter | 1 | 1 | ↑ | x | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 00 |
| 3rd parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | EP8 | 03 |
| 4th parameter | 1 | 1 | ↑ | x | EP7 | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0 | 1F |
| Description | This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.   | | | | | | | | | | | | |

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**Restriction**

SP [8:0] always must be equal to or less than EP [8:0].

1. GCM[7:0]= 70h : 480x864
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 863(035Fh)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)
2. GCM[7:0]= 6Bh : 480x854
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 853(0355h)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)
3. GCM[7:0]= 50h : 480x800
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 799(031Fh)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)
4. GCM[7:0]= 28h : 480x720
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 719(02CFh)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)
5. GCM[7:0]= 00h : 480x640
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 639(027Fh)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)
6. GCM[7:0]= FEh : 480x360
   MV(36h-B5)=0 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 359(0167h)
   MV(36h-B5)=1 : Parameter range : 0 ≦ SP[8:0] ≦ EP[8:0] ≦ 479(01DFh)

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | SC[8:0] | EC[8:0](36h-B5=0) |
| Power On Sequence | 0000h | 031Fh |
| SW Reset | 0000h | 031Fh |
| HW Reset | 0000h | 031Fh |

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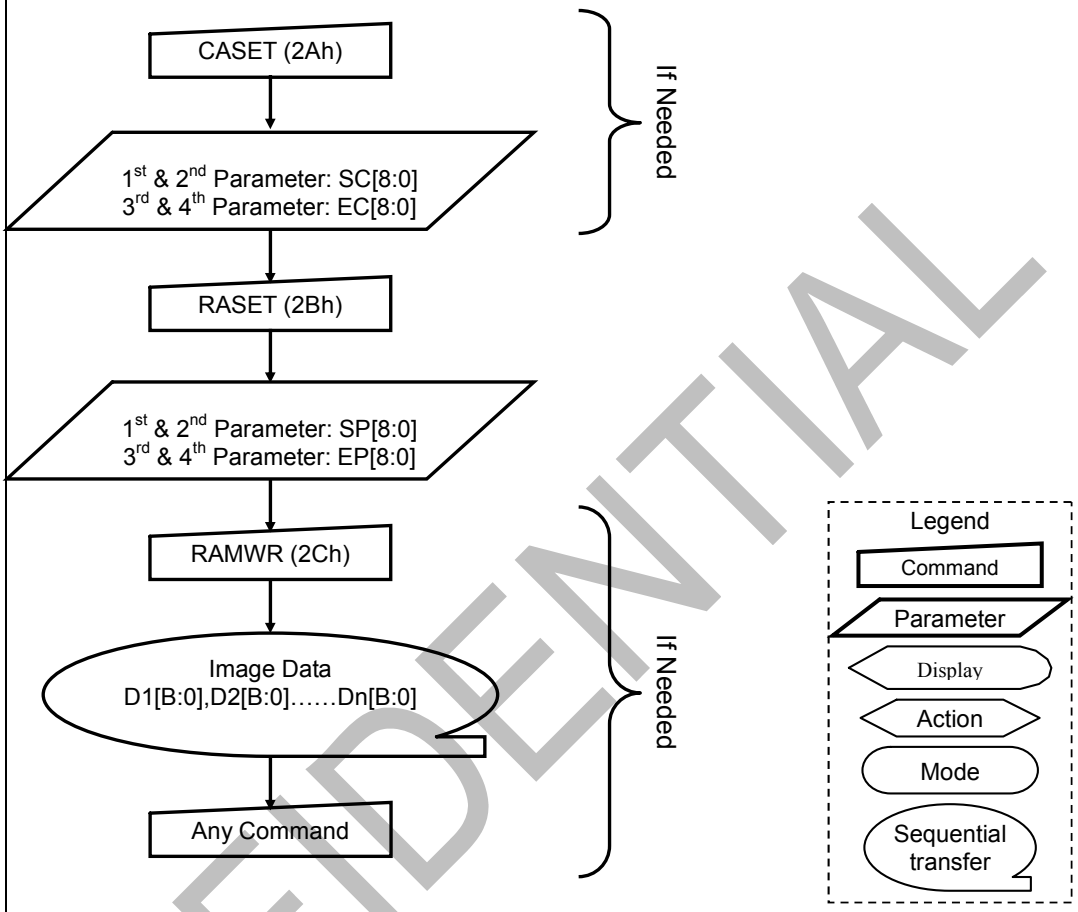
Flow chart




Note : B=23

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**RAMWR (2C00h): Memory Write**

| 2C00H | RAMWR (Memory Write) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | xx | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C |
| 1st pixel data | 1 | 1 | ↑ | D1[24..8] | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | |
| : | 1 | 1 | ↑ | Dx[24..8] | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | |
| Nth pixel data | 1 | 1 | ↑ | Dn[24..8] | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | |
| Description | This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.<br><br>If MV(36h-B5) = 0:<br>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.<br><br>If MV(36h-B5) = 1:<br>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. | | | | | | | | | | | | |
| Restriction | A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations. | | | | | | | | | | | | |

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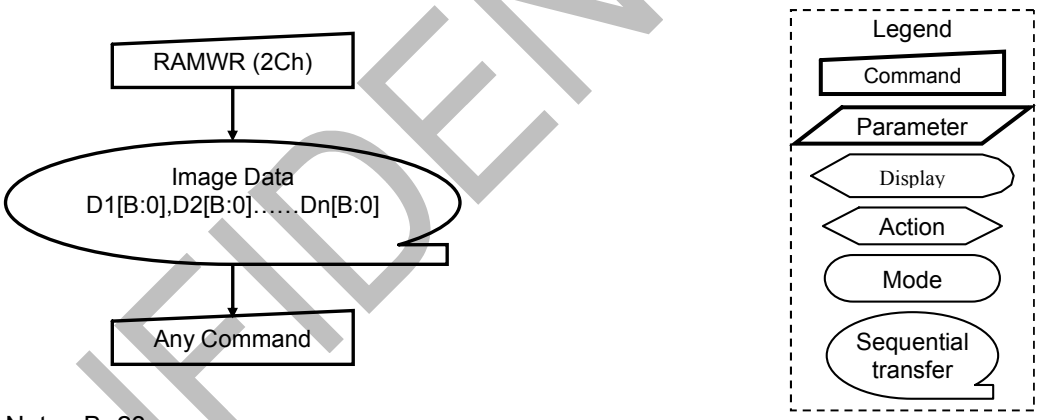
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| SW Reset | Contents of memory is not cleared |
| HW Reset | Contents of memory is not cleared |

**Flow chart**




Note : B=23

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**RAMRD (2E00h): Memory Read**

| 2E00H | RAMRD (Memory Read) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | D1[24..8] | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | |
| : | 1 | ↑ | 1 | Dx[24..8] | Dx7 | Dx6 | Dx5 | Dx4 | Dx3 | Dx2 | Dx1 | Dx0 | |
| (N+1)th parameter | 1 | ↑ | 1 | Dn[24..8] | Dn7 | Dn6 | Dn5 | Dn4 | Dn3 | Dn2 | Dn1 | Dn0 | |
| Description | This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.<br><br>If MV(36h-B5) = 0:<br>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.<br><br>If MV(36h-B5) = 1:<br>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

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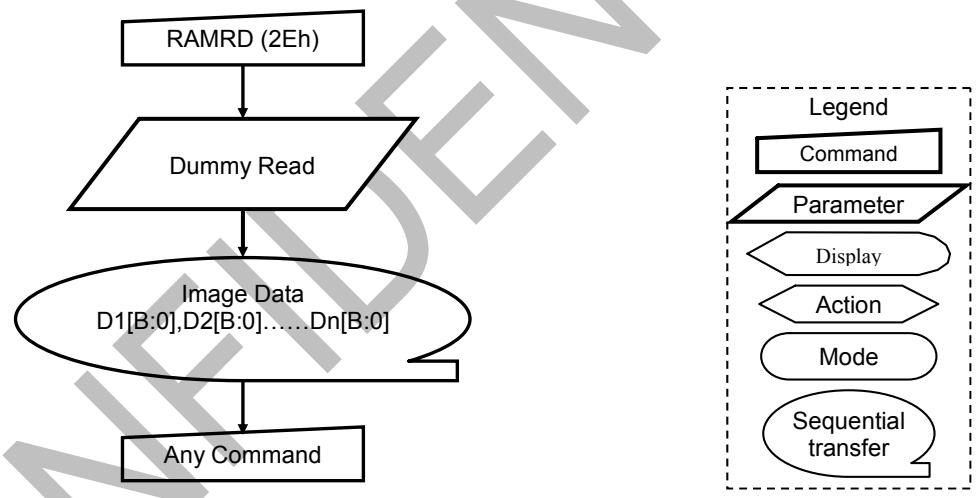
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| SW Reset | Contents of memory is not cleared |
| HW Reset | Contents of memory is not cleared |

**Flow chart**




Note : B=23

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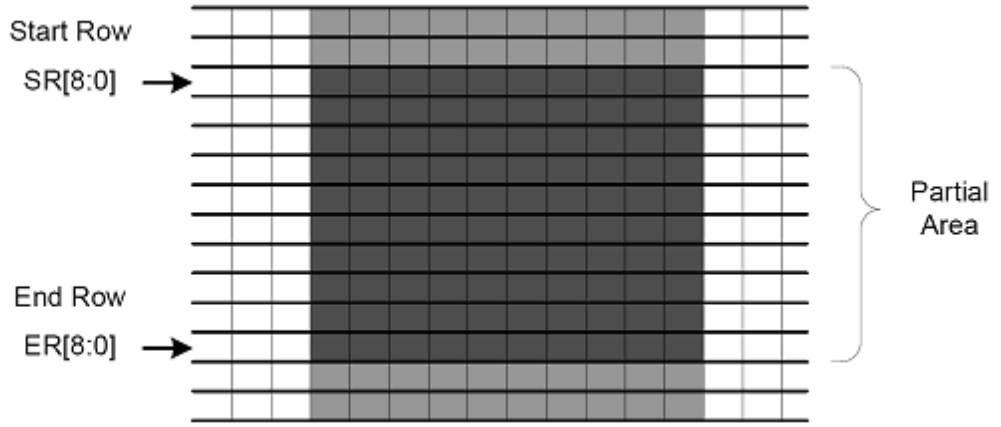
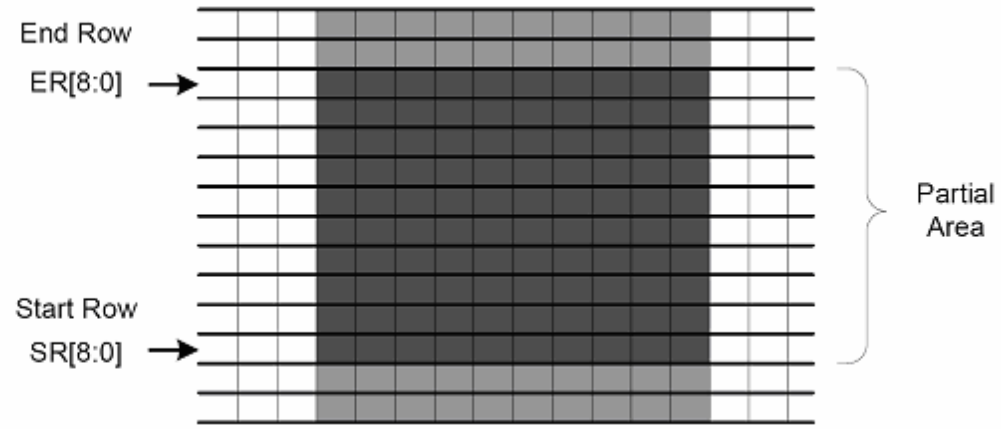
**PTLAR (3000h): Partial Area**

| 3000H | PTLAR (Partial Area) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SR8 | 00 |
| 2nd parameter | 1 | 1 | ↑ | x | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | 00 |
| 3rd parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ER8 | 03 |
| 4th parameter | 1 | 1 | ↑ | x | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | 1F |
| Description | This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory.<br><br>-If End Row > Start Row, when ML(36h-B4) ='0'<br>  <br><br>-If End Row > Start Row, when ML(36h-B4) ='1'<br>  <br> | | | | | | | | | | | | | |

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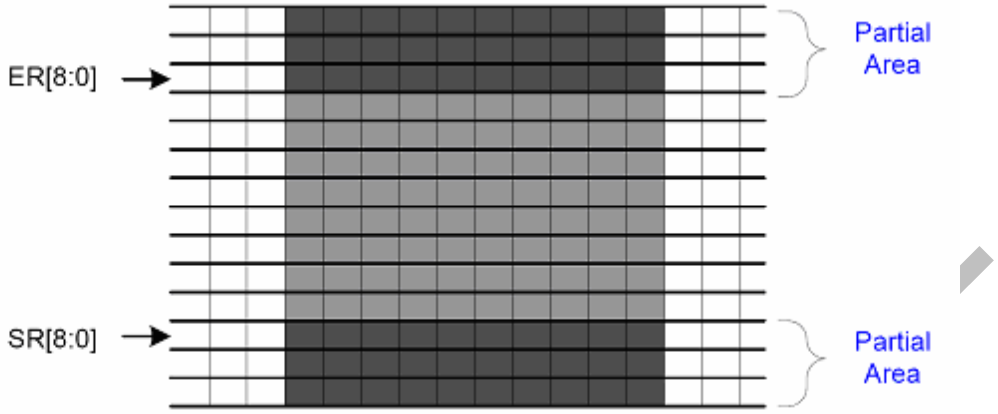
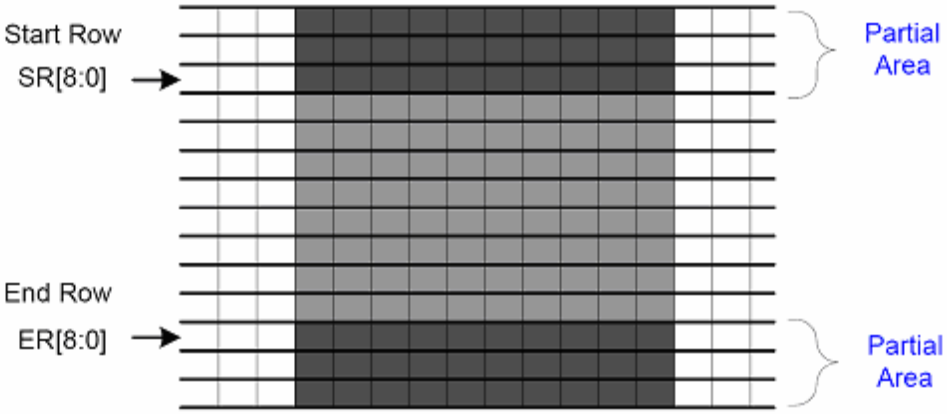
<table>
<tr>
<td></td>
<td>
-If End Row < Start Row, when ML(36h-B4) =’0’<br>


<br>
-If End Row < Start Row, when ML(36h-B4) =’1’<br>


<br>
-If End Row = Start Row then the Partial Area will be one row deep.
</td>
</tr>
<tr>
<td>Restriction</td>
<td>
CGM[7:0] = ”70h” (480 x 864): 0 ≦ SR[15:0], ER[15:0] ≦ 863 (035Fh), |ER–SR| ≦ 863 (035Fh)<br>
CGM[7:0] = ”6Bh” (480 x 854): 0 ≦ SR[15:0], ER[15:0] ≦ 853 (0355h), |ER–SR| ≦ 853 (0355h)<br>
CGM[7:0] = ”50h” (480 x 800): 0 ≦ SR[15:0], ER[15:0] ≦ 799 (031Fh), |ER–SR| ≦ 799 (031Fh)<br>
CGM[7:0] = ”28h” (480 x 720): 0 ≦ SR[15:0], ER[15:0] ≦ 719 (02CFh), |ER–SR| ≦ 719 (02CFh)<br>
CGM[7:0] = ”00h” (480 x 640): 0 ≦ SR[15:0], ER[15:0] ≦ 639 (027Fh), |ER–SR| ≦ 639 (027Fh)<br>
CGM[7:0] = ”FEh” (480 x 360): 0 ≦ SR[15:0], ER[15:0] ≦ 359 (0167h), |ER–SR| ≦ 359 (0167h)
</td>
</tr>
</table>

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**Register Availability**

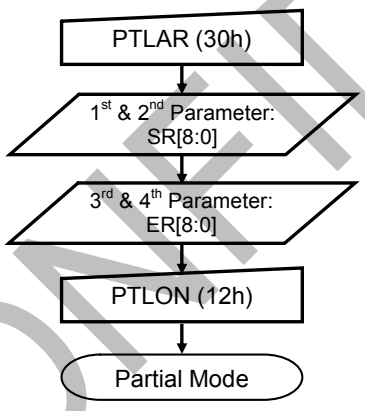
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

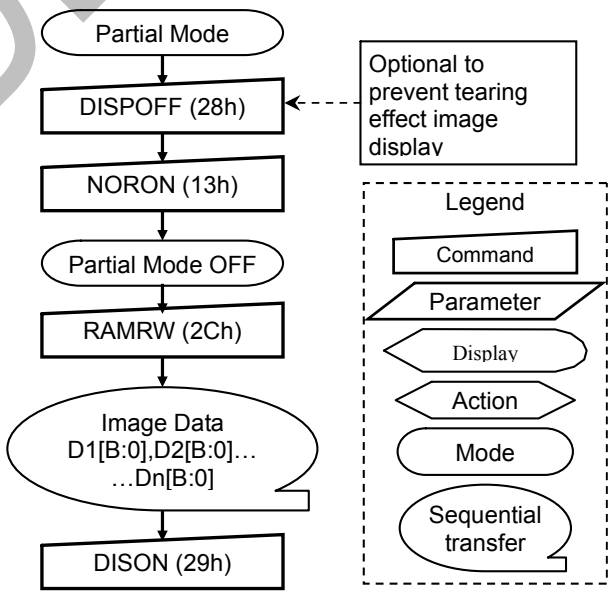
| Status | Default Value | |
|---|---|---|
| | SR[8:0] | ER[8:0] |
| Power On Sequence | 0000h | 031Fh |
| SW Reset | 0000h | 031Fh |
| HW Reset | 0000h | 031Fh |

**Flow chart**

1. To Enter Partial Mode




2. To Exit Partial Mode




Note : B=23

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**TEOFF (3400h): Tearing Effect Line OFF**

| 3400H | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command turns off the display module's Tearing Effect output signal on the TE signal line. | | | | | | | | | | | | |
| Restriction | This command has no effect when the Tearing Effect output is already off. | | | | | | | | | | | | |

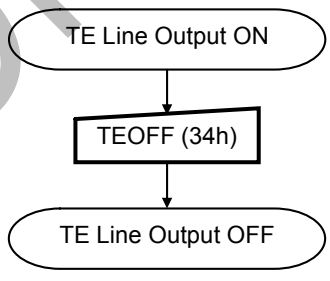
Register Availability

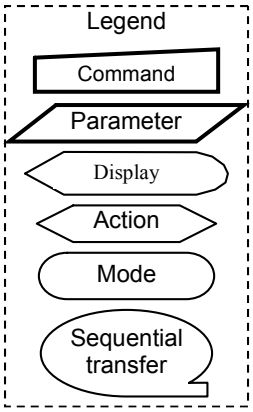
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OFF |
| SW Reset | OFF |
| HW Reset | OFF |

Flow Chart

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**TEON (3500h): Tearing Effect Line ON**

| 3500H | TEON (Tearing Effect Line ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM | 00 |
| Description | This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).<br>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.<br>If TELOM = 0:<br>The Tearing Effect Output line consists of V-Blanking information only.<br> <br>If TELOM = 1:<br>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.<br> <br>***The Tearing Effect Output line shall be active low when the display module is in Sleep mode.*** | | | | | | | | | | | | |
| Restriction | This command has no effect when Tearing Effect output is already ON. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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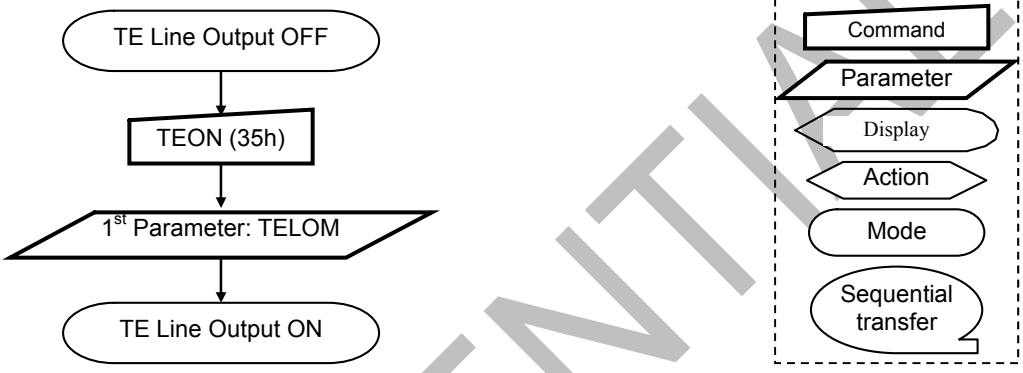
**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | OFF |
| SW Reset | OFF |
| HW Reset | OFF |

**Flow Chart**

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**MADCTR (3600h): Memory Data Access Control**

<table>
<tr><th>3600H</th><th colspan="12">MADCTR (Memory Data Access Control)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D24-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.<br><br>
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>B7</td><td>MY</td><td>Row Address Order</td><td>‘1’ = Bottom to Top<br>‘0’ = Top to Bottom</td></tr>
<tr><td>B6</td><td>MX</td><td>Column Address Order</td><td>‘1’ = Right to Left<br>‘0’ = Left to Right</td></tr>
<tr><td>B5</td><td>MV</td><td>Row/Column Order (MV)</td><td>‘1’ = Row/column exchange<br>‘0’ = Normal</td></tr>
<tr><td>B4</td><td>ML</td><td>Vertical Refresh Order</td><td>‘0’ =LCD Refresh Top to Bottom<br>‘1’ =LCD Refresh Bottom to Top</td></tr>
<tr><td>B3</td><td>RGB</td><td>RGB/BGR Order</td><td>‘1’ =BGR, “0”=RGB</td></tr>
<tr><td>B2</td><td>MH</td><td>Horizontal Refresh Order</td><td>‘0’ =LCD Refresh Left to Right<br>‘1’ =LCD Refresh Right to Left</td></tr>
<tr><td>B1</td><td>H_FLIP</td><td>Horizontal Flip</td><td>‘0’ = Normal display<br>‘1’ = Flipped display</td></tr>
<tr><td>B0</td><td>V_FLIP</td><td>Vertical Flip</td><td>‘0’ = Normal display<br>‘1’ = Flipped display</td></tr>
</table></td></tr>
</table>

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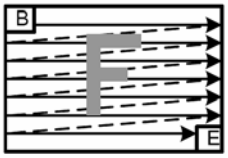
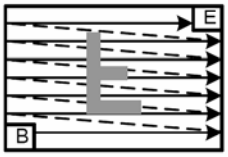
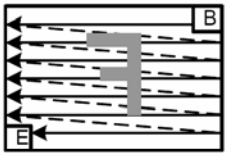
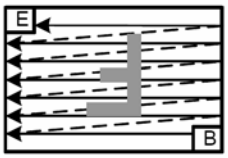
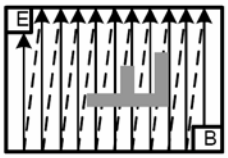
| B5 | B6 | B7 | Image in Frame Memory |
|---|---|---|---|
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |

| B5 | B6 | B7 | Image in Frame Memory |
|---|---|---|---|
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 |  |

B3 = 0

B3 = 1

| | |
|---|---|
| Restriction | |

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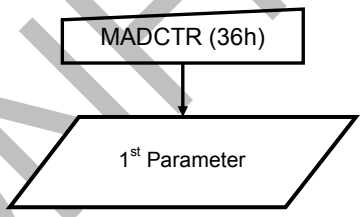
**Register Availability**

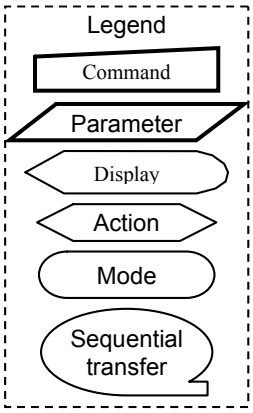
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | No Change |
| HW Reset | 00h |

**Flow chart**

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**IDMOFF (3800h): Idle Mode Off**

| 3800H | IDMOFF (Idle Mode Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command causes the display module to exit Idle mode. | | | | | | | | | | | | |
| Restriction | This command has no effect when the display module is not in Idle mode. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Idle Mode Off |
| SW Reset | Idle Mode Off |
| HW Reset | Idle Mode Off |

Flow Chart

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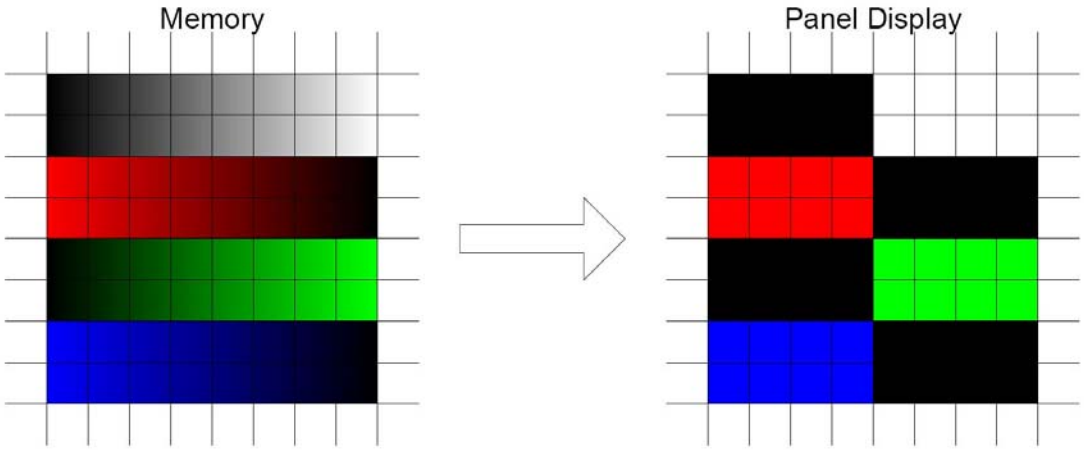
**IDMON (3900h): Enter_idle_mode**

| 3900H | Enter_idle_mode | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 |
| Parameter | NO PARAMETER | | | | | | | | | | | | |
| Description | This command causes the display module to enter Idle Mode.<br>In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory. | | | | | | | | | | | | |
| Restriction | This command has no effect when module is already in idle on mode. | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |




| Color | R7 R6 R5 R4 R3 R2 R1 R0 | G7 G6 G5 G4 G3 G2 G1 G0 | B7 B6 B5 B4 B3 B2 B1 B0 |
|---|---|---|---|
| Black | 0XXXXXXX | 0XXXXXXX | 0XXXXXXX |
| Blue | 0XXXXXXX | 0XXXXXXX | 1XXXXXXX |
| Red | 1XXXXXXX | 0XXXXXXX | 0XXXXXXX |
| Magenta | 1XXXXXXX | 0XXXXXXX | 1XXXXXXX |
| Green | 0XXXXXXX | 1XXXXXXX | 0XXXXXXX |
| Cyan | 0XXXXXXX | 1XXXXXXX | 1XXXXXXX |
| Yellow | 1XXXXXXX | 1XXXXXXX | 0XXXXXXX |
| White | 1XXXXXXX | 1XXXXXXX | 1XXXXXXX |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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Default

| Status | Default Value |
|---|---|
| Power On Sequence | Idle Mode Off |
| SW Reset | Idle Mode Off |
| HW Reset | Idle Mode Off |

Flow Chart

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**COLMOD (3A00h): Interface Pixel Format**

| 3A00H | COLMOD (Interface Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A |
| 1st parameter | 1 | 1 | ↑ | x | 0 | D6 | D5 | D4 | 0 | D2 | D1 | D0 | 66 |

Description

This command sets the pixel format for the RGB image data used by the interface.

Bits D[6:4] – DPI Pixel Format Definition

Bits D[2:0] – DBI Pixel Format Definition

Bits D7 and D3 are not used.

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.

| Control Interface Color Format | D6/D2 | D5/D1 | D4/D0 |
|---|---|---|---|
| Not defined | 0 | 0 | 0 |
| Not defined | 0 | 0 | 1 |
| Not defined | 0 | 1 | 0 |
| Not defined | 0 | 1 | 1 |
| Not defined | 1 | 0 | 0 |
| 16bit/pixel (65,536 colors) | 1 | 0 | 1 |
| 18bit/pixel (262,144 colors) | 1 | 1 | 0 |
| 24bit/pixel (16.7M colors) | 1 | 1 | 1 |

Restriction

There is no visible effect until the Frame Memory is written to.

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 66h |
| SW Reset | No Change |
| HW Reset | 66h |

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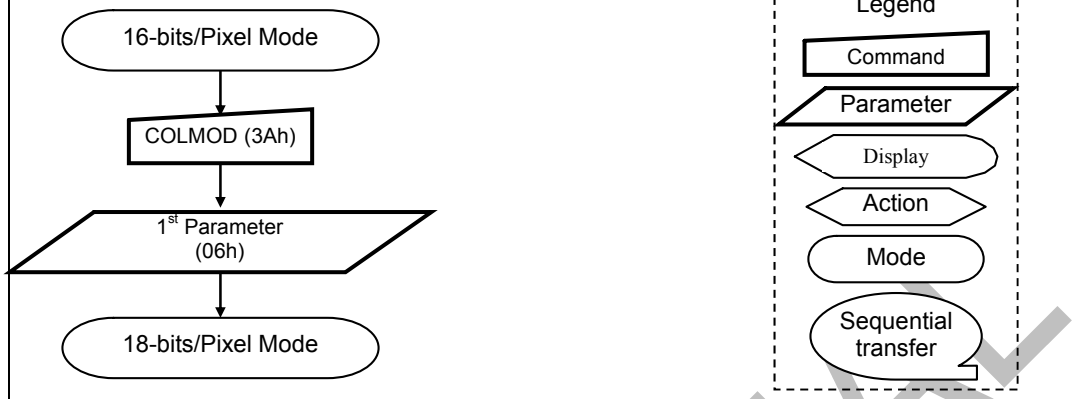
Flow chart

Example :

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**RAMWRC(3C00h) : Write_Memory_Continue**

| 3C00H | Write_Memory_Continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C |
| 1st parameter | 1 | 1 | ↑ | D1[24..8] | D1[7] | D1[6] | D1[5] | D1[4] | D1[3] | D1[2] | D1[1] | D1[0] | |
| Xst parameter | 1 | 1 | ↑ | Dx[24..8] | Dx[7] | Dx[6] | Dx[5] | Dx[4] | Dx[3] | Dx[2] | Dx[1] | Dx[0] | |
| Nst parameter | 1 | 1 | ↑ | Dn[24..8] | Dn[7] | Dn[6] | Dn[5] | Dn[4] | Dn[3] | Dn[2] | Dn[1] | Dn[0] | |

**Description**

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If MV(36h-B5) = 0:

Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If MV(36h-B5) = 1:

Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

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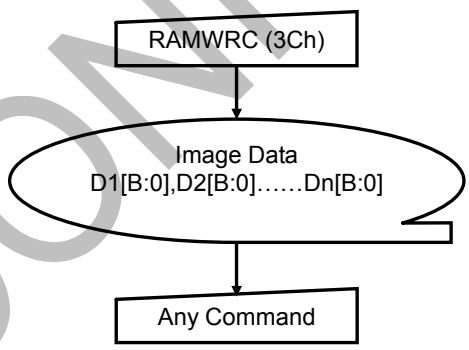
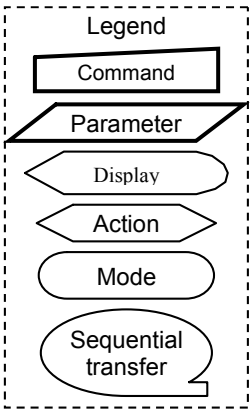
<table>
<tr><td></td><td>Frame Memory Access and Interface setting (B3h), WEMODE=1<br>When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.</td></tr>
<tr><td>Restriction</td><td>A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr>
<tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td> 



<br>Note : B = 23</td></tr>
</table>

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**RAMRDC(3E00h) : Read_Memory_Continue**

| 3E00H | Read_Memory_Continue | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D24-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | D1[24..8] | D1[7] | D1[6] | D1[5] | D1[4] | D1[3] | D1[2] | D1[1] | D1[0] | |
| Xst parameter | 1 | ↑ | 1 | Dx[24..8] | Dx[7] | Dx[6] | Dx[5] | Dx[4] | Dx[3] | Dx[2] | Dx[1] | Dx[0] | |
| Nst parameter | 1 | ↑ | 1 | Dn[24..8] | Dn[7] | Dn[6] | Dn[5] | Dn[4] | Dn[3] | Dn[2] | Dn[1] | Dn[0] | |
| Description | This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.<br><br>If MV(36h-B5) = 0:<br>Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.<br><br>If MV(36h-B5) B5 = 1:<br>Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command. | | | | | | | | | | | | |
| Restriction | A Memory Read should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMRD(2Eh) and any following RAMRDC(3Eh) commands is written to undefined locations. | | | | | | | | | | | | |

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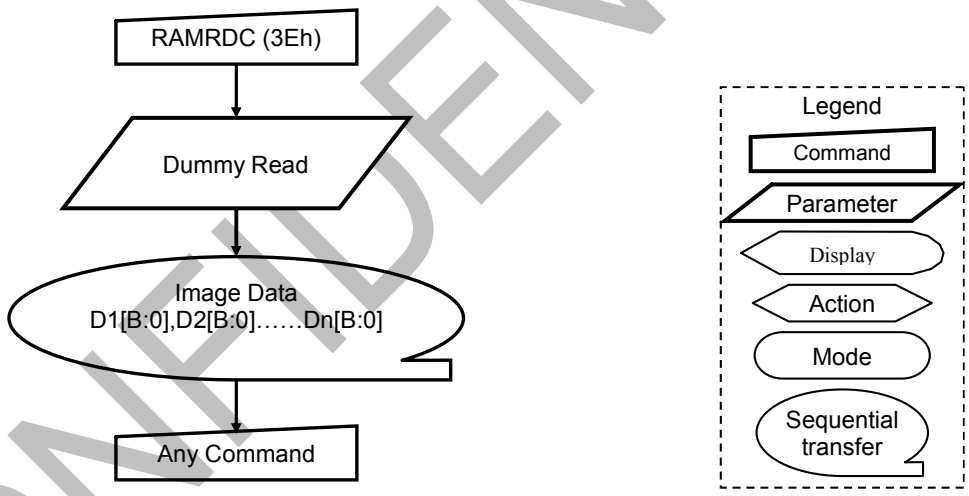
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| SW Reset | Contents of memory is not cleared |
| HW Reset | Contents of memory is not cleared |

**Flow chart**




Note : B=23

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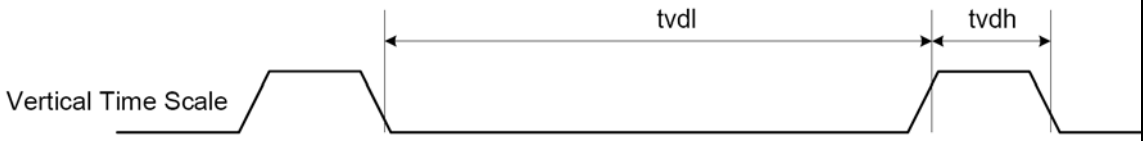
**STESL(4400h) : Set_Tear_Scanline**

| 4400H | STESL(Set_Tear_Scanline) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 |
| 1st parameter | 1 | 1 | ↑ | xx | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STS[8] | 00 |
| 2nd parameter | 1 | 1 | ↑ | xx | STS[7] | STS[6] | STS[5] | STS[4] | STS[3] | STS[2] | STS[1] | STS[0] | 00 |
| Description | This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.<br>  <br><br>The Tearing Effect Output line shall be active low when the display module is in Sleep mode. | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | STS[8:0]=9'h000 |
| SW Reset | No change |
| HW Reset | STS[8:0]=9'h000 |

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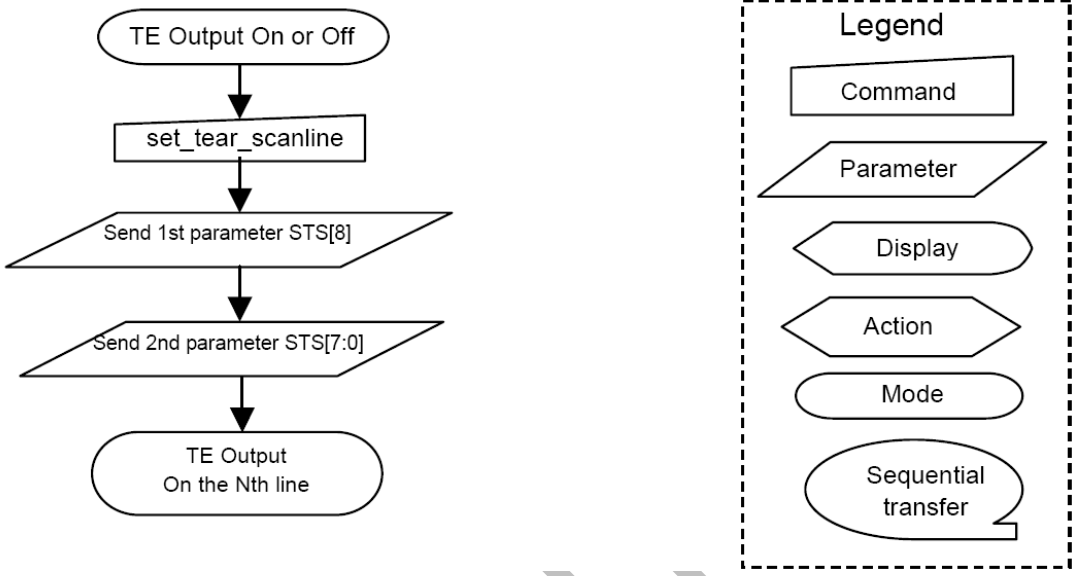
| | |
|---|---|
| Flow Chart |  |



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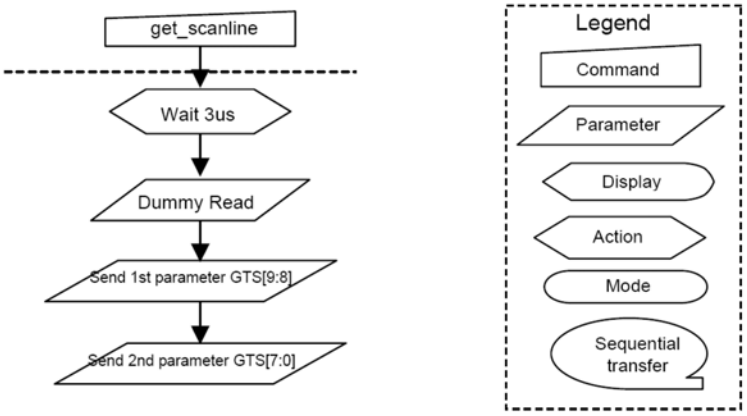
**GSL (4500h) : Get_Scanline**

| 4500H | GSL(Get_Scanline) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GTS[8] | 0x |
| 3rd parameter | 1 | ↑ | 1 | xx | GTS[7] | GTS[6] | GTS[5] | GTS[4] | GTS[3] | GTS[2] | GTS[1] | GTS[0] | xx |
| Description | The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.<br>When in Sleep Mode, the value returned by get_scanline is undefined. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Flow Chart

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**DSTBON (4F00h): Deep Standby Mode On**

| 4F00H | DSTBON(Deep Standby Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DSTB | 00 |
| Description | This command is used to enter deep standby mode.<br>DSTB=”1”, enter deep standby mode.<br>Notes:<br>1. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX. | | | | | | | | | | | | |
| Restriction | There is no visible effect until the Frame Memory is written to. | | | | | | | | | | | | |

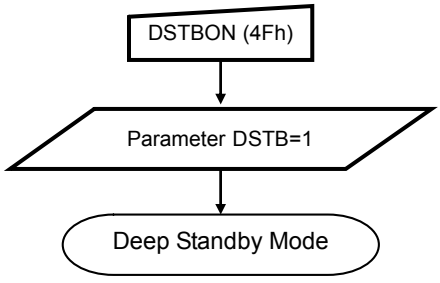
Register Availability

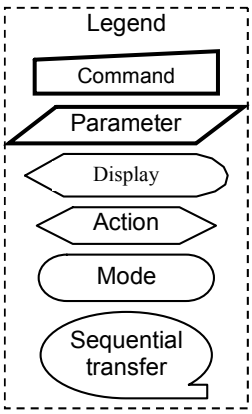
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow chart

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**WRPFD(50h) : Write Profile Value for Display**

| 50H | WRPFD | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | X | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 |
| 1st parameter | 1 | ↑ | 1 | X | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | V017 | V016 | V015 | V014 | V013 | V012 | V011 | V010 | FF |
| 3rd parameter | 1 | ↑ | 1 | xx | V027 | V026 | V025 | V024 | V023 | V022 | V021 | V020 | FF |
| nth parameter | 1 | ↑ | 1 | xx | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 15th parameter | 1 | ↑ | 1 | xx | V157 | V156 | V155 | V154 | V153 | V152 | V151 | V150 | FF |
| 16th parameter | 1 | ↑ | 1 | xx | V167 | V166 | V165 | V164 | V163 | V162 | V161 | V160 | FF |
| Description | This command is used to define profile values for display. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | FFh |
| SW Reset | FFh |
| HW Reset | FFh |

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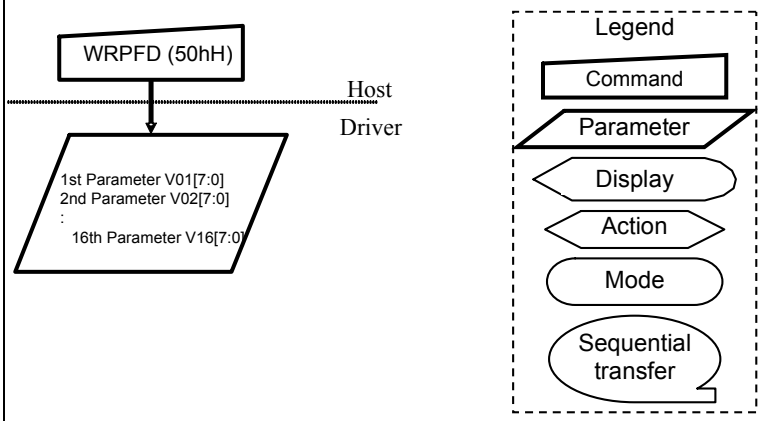
| | |
|---|---|
| Flow Chart |  |



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**WRDISBV (5100h): Write Display Brightness**

| 5100H | WRDISBV | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 |
| 1st parameter | 1 | 1 | ↑ | x | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | 00 |

**Description**

This command is used to adjust brightness value.

In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

| DBV[7:0] | Brightness (ratio) | Brightness (%) |
|---|---|---|
| 00h | 0/256 | 0% |
| 01h | 2/256 | 0.78125% |
| : | : | : |
| FEh | 255/256 | 99.609375% |
| FFh | 256/256 | 100% |

**Restriction**

The display supplier cannot use this command for tuning

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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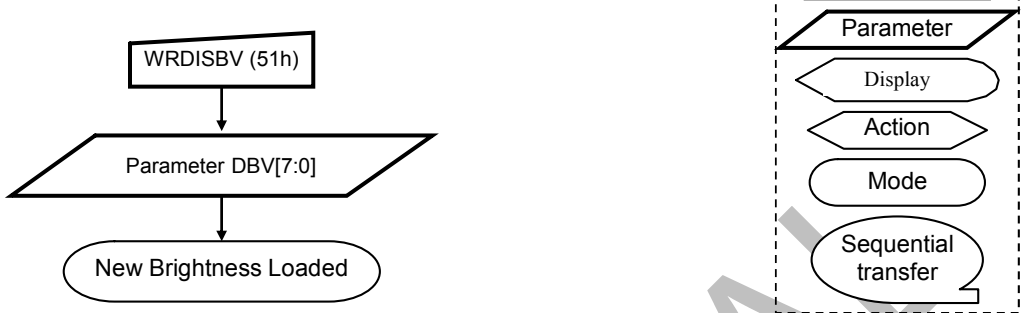
| | |
|---|---|
| Flow chart |  |



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**RDDISBV (5200h): Read Display Brightness**

| 5200H | RDDISBV | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | X |
| 2nd parameter | 1 | ↑ | 1 | x | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | 00 |
| Description | This command returns brightness value.<br>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

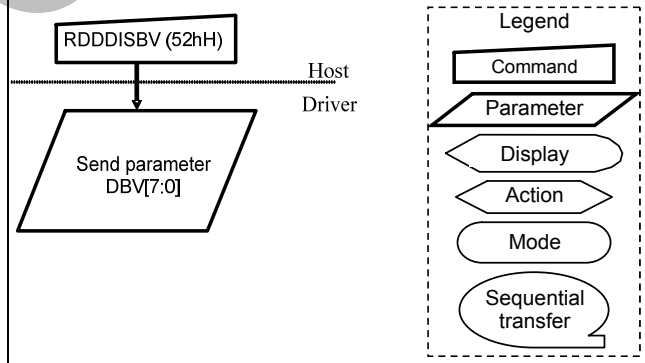
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow Chart

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**WRCTRLD (5300h): Write CTRL Display**

| 5300H | WRCTRLD | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | BCTRL | A | DD | BL | DB | G | 00 |

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Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

| BCTRL | DESCRIPTION LEDPWM Pin | DESCRIPTION LEDPWM Pin |
|---|---|---|
| 0 | Off,<br>DBV[7:0] and KBV[7:0] are 00h. | LEDPWPOL="0": keep low (0%)<br>LEDPWPOL="1": keep high (0%) |
| 1 | On,<br>DBV[7:0] and KBV[7:0] are active | LEDPWPOL="0": PWM output (high level is duty)<br>LEDPWPOL="1": PWM output (low level is duty) |

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

| A | DESCRIPTION | PWM duty for LEDPWM Pin |
|---|---|---|
| 0 | Off | By DBV[7:0] of command "WRDISBV (5100h)" |
| 1 | On | By LABC block |

DD: Display Dimming Control On/Off

| DD | DESCRIPTION |
|---|---|
| 0 | Display dimming is off |
| 1 | Display dimming is on |

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

| BL | DESCRIPTION | LEDON Pin |
|---|---|---|
| 0 | Off | LEDONPOL="0": keep low (non-lit)<br>LEDPWPOL="1": keep high (non-lit) |
| 1 | On | LEDPWPOL="0": keep high (lit)<br>LEDPWPOL="1": PWM output (lit) |

DB: Display Brightness Manual/Automatic

| DB | DESCRIPTION |
|---|---|
| 0 | Manual, the user has to use this setting for manual adjustment of the brightness to have an effect. |
| 1 | Automatic, information about the used brightness is included in the active profile. |

*Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.*

G: Gamma Curve Manual/Automatic

| G | DESCRIPTION |
|---|---|
| 0 | Manual, by GAMSET-command |
| 1 | Automatic, information about the used gamma is included in the active profile. |

The *dimming* function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

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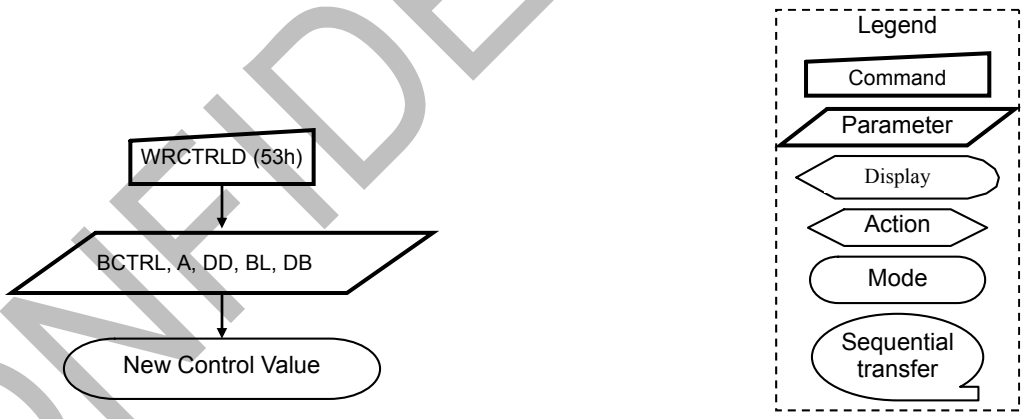
<table>
<tr><td>Restriction</td><td>The display supplier cannot use this command for tuning</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td> 
</td></tr>
</table>

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**RDCTRLD (5400h): Read CTRL Display Value**

| 5400H | RDCTRLD | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | X |
| 2nd parameter | 1 | ↑ | 1 | x | 0 | 0 | BCTRL | A | DD | BL | DB | G | 00 |

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Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

| BCTRL | DESCRIPTION LEDPWM Pin | DESCRIPTION LEDPWM Pin |
|---|---|---|
| 0 | Off,<br>DBV[7:0] and KBV[7:0] are 00h. | LEDPWPOL="0": keep low (0%)<br>LEDPWPOL="1": keep high (0%) |
| 1 | On,<br>DBV[7:0] and KBV[7:0] are active | LEDPWPOL="0": PWM output (high level is duty)<br>LEDPWPOL="1": PWM output (low level is duty) |

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

| A | DESCRIPTION | PWM duty for LEDPWM Pin |
|---|---|---|
| 0 | Off | By DBV[7:0] of command "WRDISBV (5100h)" |
| 1 | On | By LABC block |

DD: Display Dimming Control On/Off

| DD | DESCRIPTION |
|---|---|
| 0 | Display dimming is off |
| 1 | Display dimming is on |

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

| BL | DESCRIPTION | LEDON Pin |
|---|---|---|
| 0 | Off | LEDONPOL="0": keep low (non-lit)<br>LEDPWPOL="1": keep high (non-lit) |
| 1 | On | LEDPWPOL="0": keep high (lit)<br>LEDPWPOL="1": PWM output (lit) |

DB: Display Brightness Manual/Automatic

| DB | DESCRIPTION |
|---|---|
| 0 | Manual, the user has to use this setting for manual adjustment of the brightness to have an effect. |
| 1 | Automatic, information about the used brightness is included in the active profile. |

*Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.*

G: Gamma Curve Manual/Automatic

| G | DESCRIPTION |
|---|---|
| 0 | Manual, by GAMSET-command |
| 1 | Automatic, information about the used gamma is included in the active profile. |

The *dimming* function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

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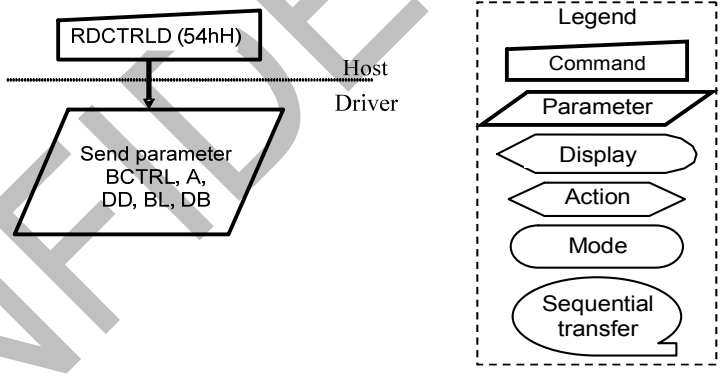
<table>
<tr><td>Restriction</td><td>The display supplier cannot use this command for tuning</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

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**WRCABC (5500h): Write Content Adaptive Brightness Control**

| 5500H | WRCABC | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 |
| 1st parameter | 1 | 1 | ↑ | x | 0 | 0 | 0 | 0 | 0 | 0 | C1 | C0 | 00 |

**Description**

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function |
|---|---|---|
| 0 | 0 | Off |
| 0 | 1 | UI Mode |
| 1 | 0 | Still Mode |
| 1 | 1 | Moving Mode |

**Restriction**

This register is synchronized with V-sync by internal circuit.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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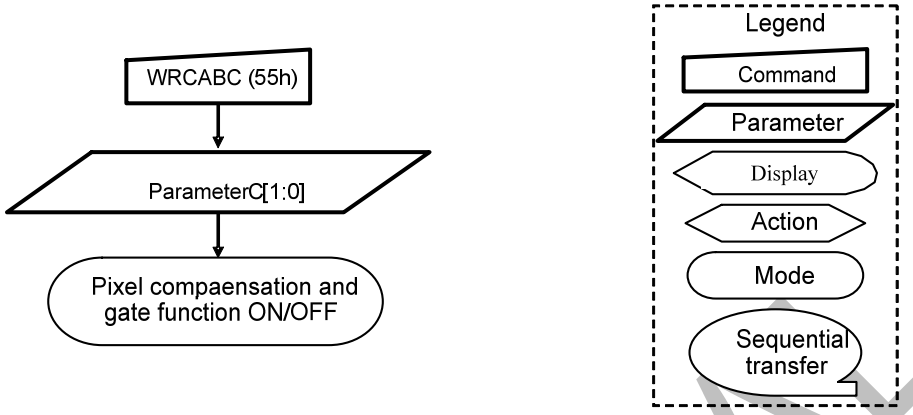
| | |
|---|---|
| Flow chart |  |



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**RDCABC (5600h): Read Content Adpative Brightness Control**

<table>
<tr><th>5600H</th><th colspan="13">RDCABC</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>56</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C1</td><td>C0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below..
<table>
<tr><th>C1</th><th>C0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Off</td></tr>
<tr><td>0</td><td>1</td><td>UI Mode</td></tr>
<tr><td>1</td><td>0</td><td>Still Mode</td></tr>
<tr><td>1</td><td>1</td><td>Moving Mode</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

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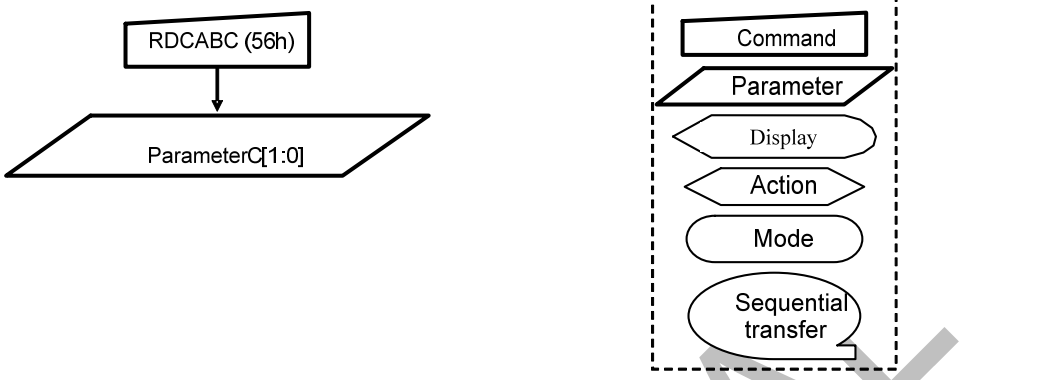
| | |
|---|---|
| Flow Chart |  |



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**WRHYSTE (5700h): Write Hystersis**

| 5700H | WRHYSTE | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 57 |
| 1st parameter | 1 | 1 | ↑ | x | I0115 | I0114 | I0113 | I0112 | I0111 | I0110 | I019 | I018 | FF |
| 2nd parameter | 1 | 1 | ↑ | x | I017 | I016 | I015 | I014 | I013 | I012 | I011 | I010 | FF |
| 3rd parameter | 1 | 1 | ↑ | x | I0215 | I0214 | I0213 | I0212 | I0211 | I0210 | I029 | I028 | FF |
| 4th parameter | 1 | 1 | ↑ | x | I027 | I026 | I025 | I024 | I023 | I022 | I021 | I020 | FF |
| : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| 28rd parameter | 1 | 1 | ↑ | x | I1515 | I1514 | I1513 | I1512 | I1511 | I1510 | I159 | I158 | FF |
| 29th parameter | 1 | 1 | ↑ | x | I157 | I156 | I155 | I154 | I153 | I152 | I151 | I150 | FF |
| 30rd parameter | 1 | 1 | ↑ | x | I1615 | I1614 | I1613 | I1612 | I1611 | I1610 | I169 | I168 | FF |
| 31th parameter | 1 | 1 | ↑ | x | I167 | I166 | I165 | I164 | I163 | I162 | I161 | I160 | FF |
| 32rd parameter | 1 | 1 | ↑ | x | D0115 | D0114 | D0113 | D0112 | D0111 | D0110 | D019 | D018 | FF |
| 33th parameter | 1 | 1 | ↑ | x | D017 | D016 | D015 | D014 | D013 | D012 | D011 | D010 | FF |
| 34rd parameter | 1 | 1 | ↑ | x | D0215 | D0214 | D0213 | D0212 | D0211 | D0210 | D029 | D028 | FF |
| 35th parameter | 1 | 1 | ↑ | x | D027 | D026 | D025 | D024 | D023 | D022 | D021 | D020 | FF |
| : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| 60rd parameter | 1 | 1 | ↑ | x | D1515 | D1514 | D1513 | D1512 | D1511 | D1510 | D159 | D158 | FF |
| 61th parameter | 1 | 1 | ↑ | x | D157 | D156 | D155 | D154 | D153 | D152 | D151 | D150 | FF |
| 62rd parameter | 1 | 1 | ↑ | x | D1615 | D1614 | D1613 | D1612 | D1611 | D1610 | D169 | D168 | FF |
| 63th parameter | 1 | 1 | ↑ | x | D167 | D166 | D165 | D164 | D163 | D162 | D161 | D160 | FF |
| Description | This command is used to define Hysteresis filter function.<br>In[15:0] defines increment values and Dn[15:0] defines decrement values.<br>Don't care about the parameter values after "65535 (FFFFh)".<br>I16[15 : 0] bits and D16[15 : 0] bits are always set to "65535 (FFFFh)" internally, if I15[15 : 0] bits and D15[15 : 0] bit are still valid and less than "65535 (FFFFh)". | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

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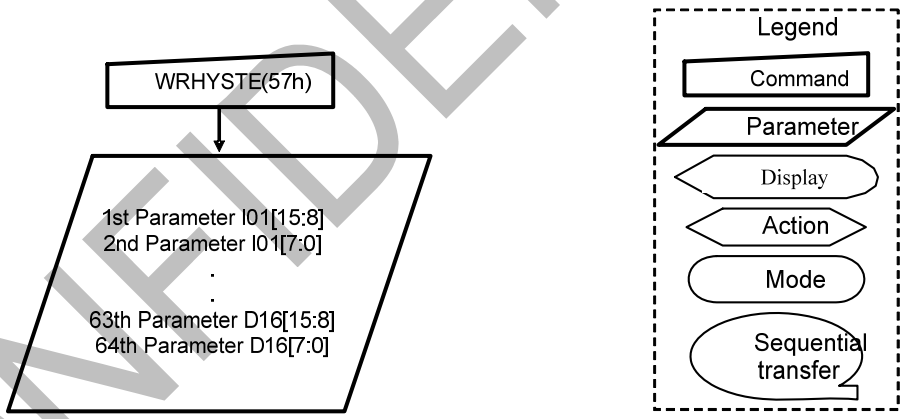
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | FFh |
| SW Reset | FFh |
| HW Reset | FFh |

**Flow chart**

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**WRGAMMASET (5800h): Write Gamma Setting**

| 5800H | WRGAMMASET | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 58 |
| 1st parameter | 1 | 1 | ↑ | x | G023 | G022 | G021 | G020 | G013 | G012 | G011 | G010 | 01 |
| 2nd parameter | 1 | 1 | ↑ | x | G043 | G042 | G041 | G040 | G033 | G032 | G031 | G030 | 01 |
| : | : | : | : | : | : | : | : | : | : | : | : | : | 01 |
| 7rd parameter | 1 | 1 | ↑ | x | G143 | G142 | G141 | G140 | G133 | G132 | G131 | G130 | 01 |
| 8th parameter | 1 | 1 | ↑ | x | G163 | G162 | G161 | G160 | G153 | G152 | G151 | G150 | 01 |

**Description**

This command is used to define gamma setting values for each luminance level.

Gamma value is defined on command “Gamma Set (2600h)”.

| Gn[3:0] | Parameter | Curve Selected |
|---|---|---|
| 01h | GC0 | Gamma Curve 1 (G=2.2) |
| 02h | GC1 | Reserved |
| 04h | GC2 | Reserved |
| 08h | GC3 | Reserved |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 01h |
| SW Reset | 01h |
| HW Reset | 01h |

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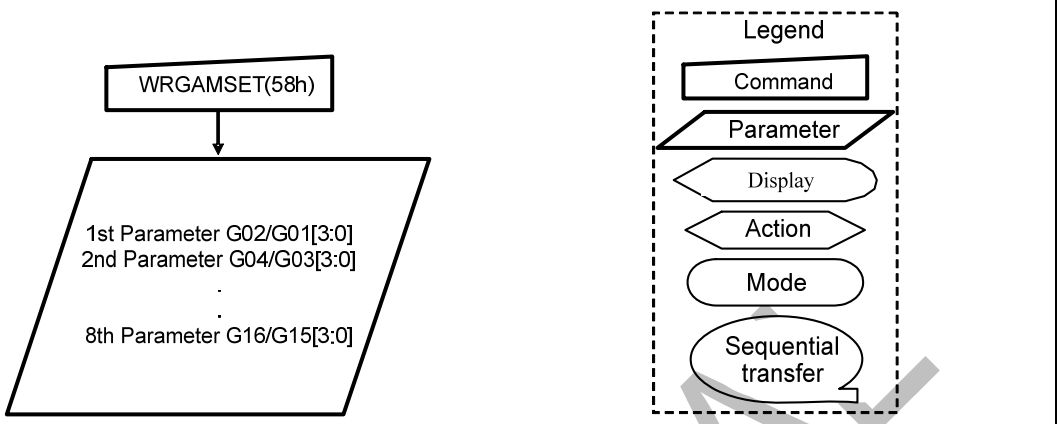
| | |
|---|---|
| Flow chart |  |



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**RDFSVM (5A00h): Read FS Value MSBs**

| 5A00H | RDFSVM | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | X |
| 2nd parameter | 1 | ↑ | 1 | x | FSV15 | FSV14 | FSV13 | FSV12 | FSV11 | FSV10 | FSV9 | FSV8 | FF |
| Description | This command returns MSBs (FSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading.<br>Another command for LSBs (FSV[7:0]). See the command "Read FS Value LSBs (5B00h)".<br>When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.<br>If *any other* commands are received between LSBs read command and MSBs read command, the *registers* for MSBs and LSBs should be released.<br>FSV[*15*:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".<br>*Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".* | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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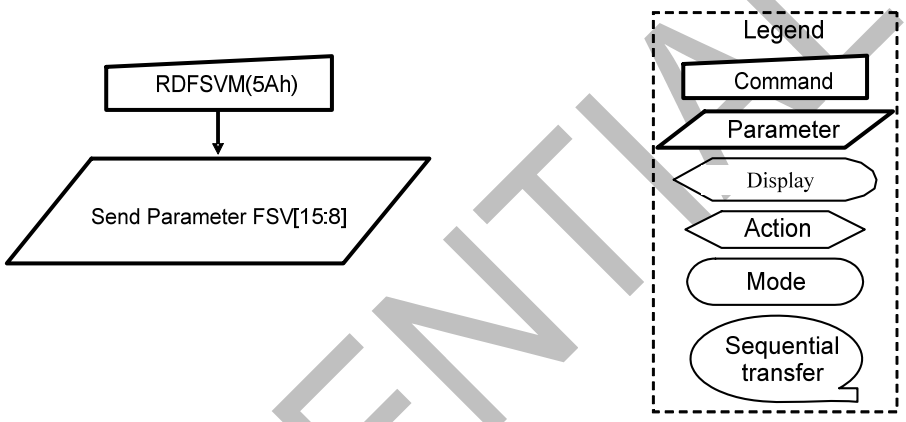
Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow Chart

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**RDFSVL (5B00h): Read FS Value LSBs**

| 5B00H | RDFSVL | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | X |
| 2nd parameter | 1 | ↑ | 1 | x | FSV7 | FSV6 | FSV5 | FSV4 | FSV3 | FSV2 | FSV1 | FSV0 | FF |
| Description | This command returns LSBs (FSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading.<br>Another command for MSBs (FSV[15:8]). See the command "Read FS Value MSBs (5A00h)".<br>When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.<br>If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.<br>FSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".<br>*Note:* Although *FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".* | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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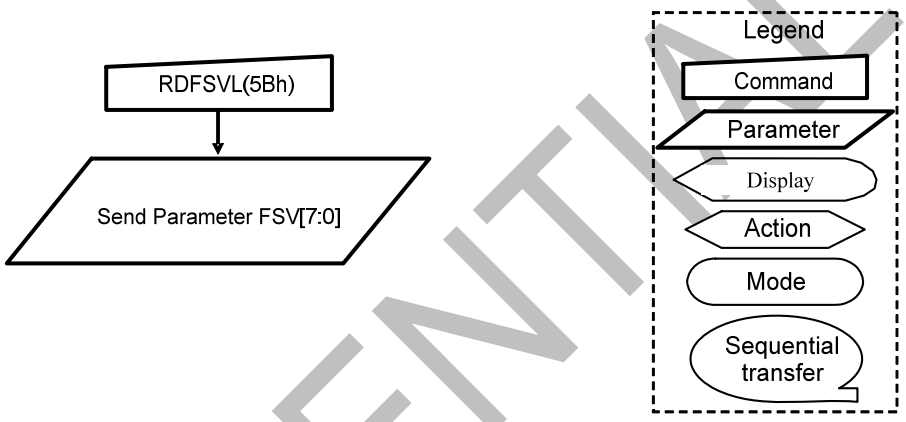
<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

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**RDMFFSVM (5C00h): Read Median Filter FS Value MSBs**

| 5C00H | RDMFFSVM | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5A |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | FFSV15 | FFSV14 | FFSV13 | FFSV12 | FFSV11 | FFSV10 | FFSV9 | FFSV8 | FF |
| Description | This command returns MSBs (FFSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the median filter.<br>Another command for LSBs (FFSV[7:0]). See the command "Read Median Filter FS Value LSBs (5D00h)".<br>When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.<br>If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.<br>FFSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".<br>*Note: Although FFSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".* | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Partial Mode On, Idle Mode Off, Sleep Out / Yes<br>Partial Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes | | | | | | | | | | | | |

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<table>
<tr><td>Default</td><td>
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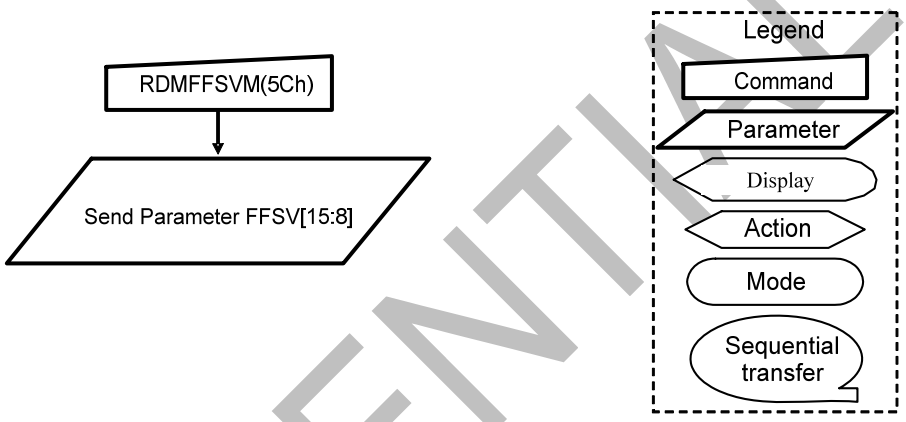
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

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**RDMFFSVL (5D00h): Read Median Filter FS Value LSBs**

| 5D00H | RDMFFSVL | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | FFSV7 | FFSV6 | FFSV5 | FFSV4 | FFSV3 | FFSV2 | FFSV1 | FFSV0 | FF |
| Description | This command returns LSBs (FDSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the median filter.<br>Another command for MSBs (FFSV[15:8]). See the command "Read Median Filter FS Value MSBs (5C00h)".<br>When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.<br>If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.<br>FFSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".<br>*Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".* | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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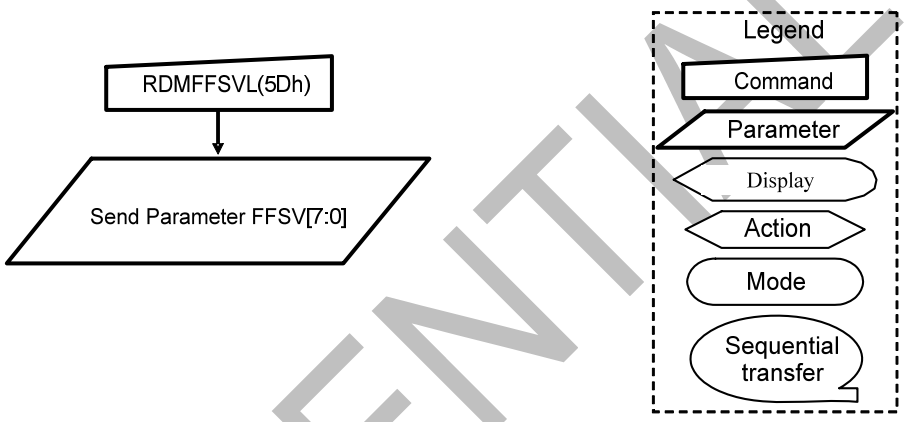
<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

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**WRCABCMB (5E00h): Write CABC Minimum Brightness**

| 5E00H | WRCABCMB | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E |
| 1st parameter | 1 | 1 | ↑ | x | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | 00 |
| Description | This command is used to set the minimum brightness value of the display for CABC function<br>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

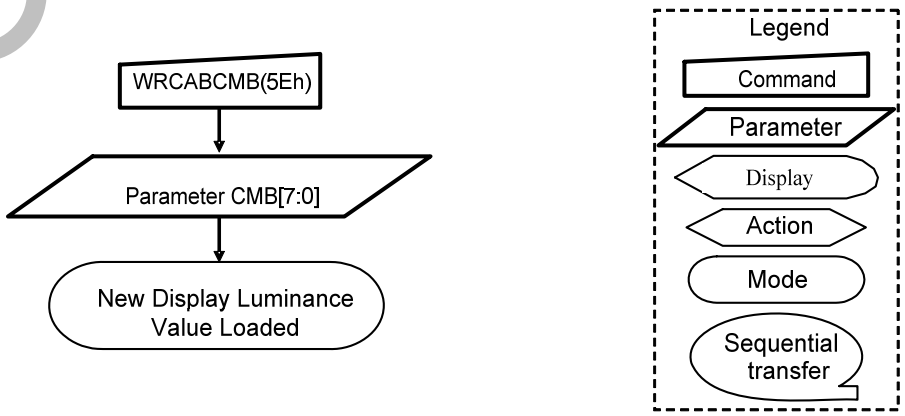
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow chart

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**RDCABCMB (5F00h): Read CABC Minimum Brightness**

| 5F00H | RDCABCMB | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F |
| 1st parameter | 1 | 1 | ↑ | x | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | 00 |
| Description | This command return the minimum brightness value of CABC function<br>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.<br>CMB[7:0] is minimum brightness forCABC specified with “WRCABCMB Write CABC minimum brightness (5Eh)” command. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

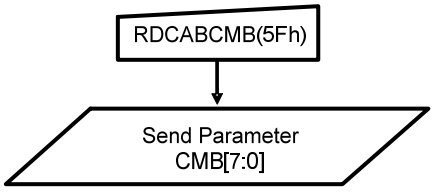
Register Availability

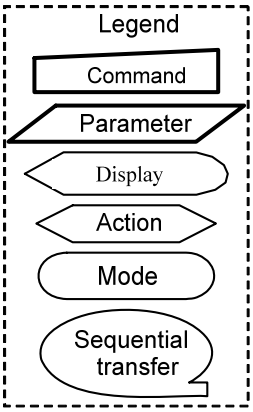
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow chart

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**WRLSCC (6500h): Write Light Sensor Compensation Coefficient Value**

| 6500H | WRLSCC | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 65 |
| 1st parameter | 1 | 1 | ↑ | x | CC15 | CC14 | CC13 | CC12 | CC11 | CC10 | CC9 | CC8 | 80 |
| 2nd parameter | 1 | 1 | ↑ | x | CC7 | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | 00 |
| Description | This command is used to send the compensation coefficient value (CC[15 : 0]).<br>Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). | | | | | | | | | | | | |
| Restriction | The display supplier cannot use this command for tuning (e.g. factory tuning, etc.). | | | | | | | | | | | | |

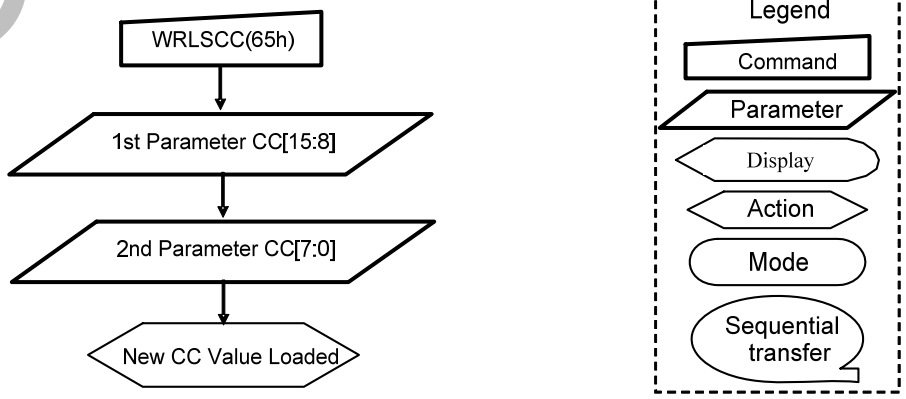
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 8000h |
| SW Reset | 8000h |
| HW Reset | 8000h |

Flow chart

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**RDLSCCM (6600h): Read Light Sensor Compensation Coefficient Value MSBs**

| 6600H | RDLSCCM | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 66 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | CC15 | CC14 | CC13 | CC12 | CC11 | CC10 | CC9 | CC8 | 80 |
| Description | This command returns MSBs of the compensation coefficient value (CC[15:8]) which is stored by “Write Light Sensor Compensation Coefficient Value (6500h)” command.<br>It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order.<br>Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are “1000 000”. | | | | | | | | | | | | |
| Restriction | The display supplier cannot use this command for tuning (e.g. factory tuning, etc.). | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 80h |
| SW Reset | 80h |
| HW Reset | 80h |

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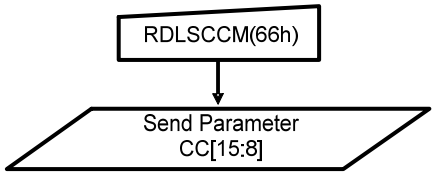
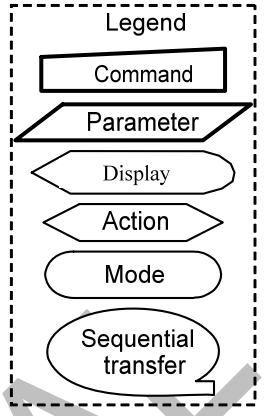
| | |
|---|---|
| Flow Chart |   |

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**RDLSCCL (6700h): Read Light Sensor Compensation Coefficient Value LSBs**

| 6700H | RDLSCCL | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 67 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | CC7 | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | 00 |
| Description | This command returns LSBs of the compensation coefficient value (CC[7:0]) which is stored by “Write Light Sensor Compensation Coefficient Value (6501h)” command.<br>It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order.<br>Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are “0000 000”. | | | | | | | | | | | | |
| Restriction | The display supplier cannot use this command for tuning (e.g. factory tuning, etc.). | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

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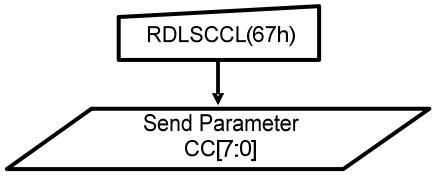
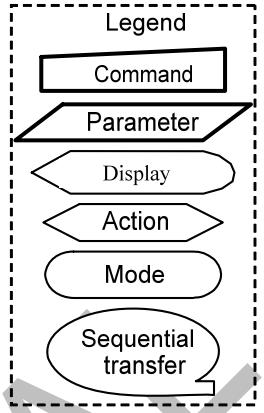
| | |
|---|---|
| Flow Chart |   |

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**RDBWLB (7000h): Read Black/White Low Bits**

| 7000H | RDBWLB | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Bkx1 | Bkx0 | Bky1 | Bky0 | Wx1 | Wx0 | Wy1 | Wy0 | 00 |
| Description | This command returns the lowest bits of black and white color characteristic.<br>Black: Bkx and Bky<br>White: Wx and Wy | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

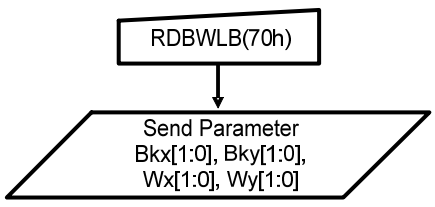
Register Availability

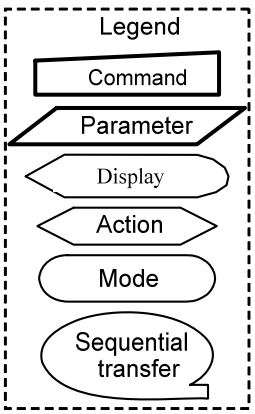
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDBkx (7100h): Read Bkx**

| 7100H | RDBkx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Bkx9 | Bkx8 | Bkx7 | Bkx6 | Bkx5 | Bkx4 | Bkx3 | Bkx2 | 00 |
| Description | This command returns the Bkx bit (Bkx[9:2]) of black color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

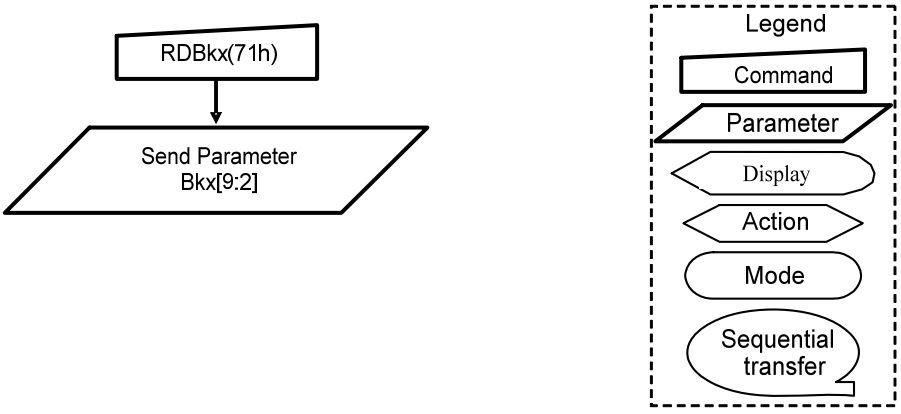
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDBky (7200h): Read Bky**

| 7200H | RDBky | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Bky9 | Bky8 | Bky7 | Bky6 | Bky5 | Bky4 | Bky3 | Bky2 | 00 |
| Description | This command returns the Bky bit (Bky[9:2]) of black color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

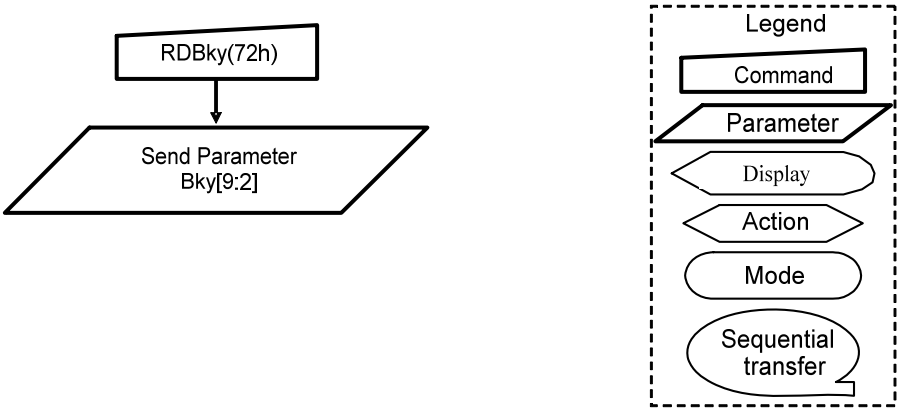
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDWx (7300h): Read Wx**

| 7300H | RDWx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Wx9 | Wx8 | Wx7 | Wx6 | Wx5 | Wx4 | Wx3 | Wx2 | 00 |
| Description | This command returns the Wx bit (Wx[9:2]) of black color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

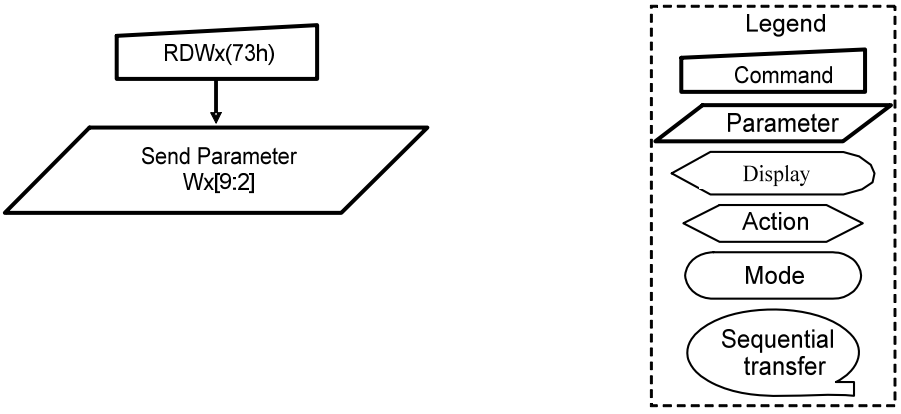
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDWy (7400h): Read Wy**

| 7400H | RDWy | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | 00 |
| Description | This command returns the Bky bit (Bky[9:2]) of black color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

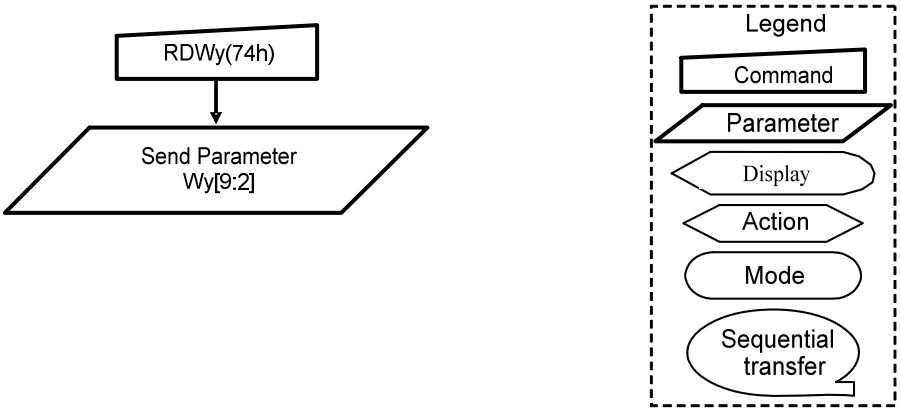
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDRGLB (7500h): Read Red/Green Low Bits**

| 7500H | RDRGLB | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 75 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Rx1 | Rx0 | Ry1 | Ry0 | Gx1 | Gx0 | Gy1 | Gy0 | 00 |

**Description**

This command returns the lowest bits of red and green color characteristic.

Red: Rx and Ry

Green: Gx and Gy

**Restriction**

-

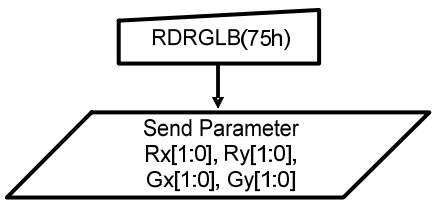
**Register Availability**

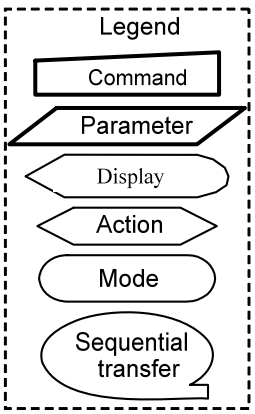
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

**Flow Chart**

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**RDRx (7600h): Read Rx**

| 7600H | RDRx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Rx9 | Rx8 | Rx7 | Rx6 | Rx5 | Rx4 | Rx3 | Rx2 | 00 |
| Description | This command returns the Rx bit (Rx[9:2]) of red color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

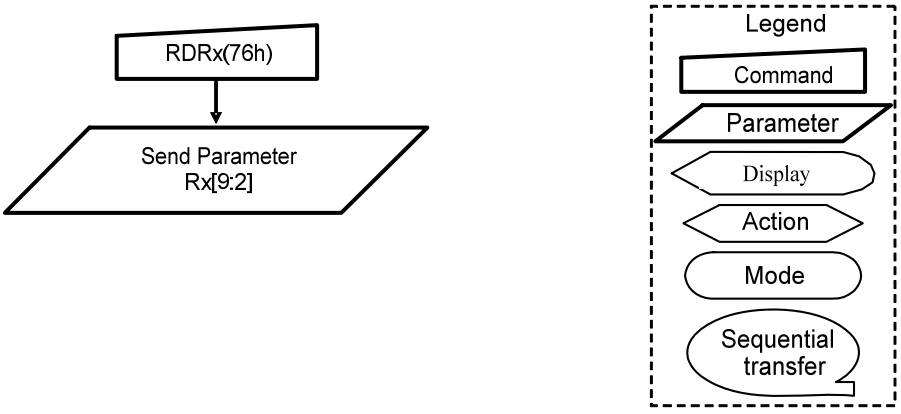
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDRy (7700h): Read Ry**

| 7700H | RDRy | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 77 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Wy9 | Wy8 | Wy7 | Wy6 | Wy5 | Wy4 | Wy3 | Wy2 | 00 |
| Description | This command returns the Ry bit (Ry[9:2]) of red color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

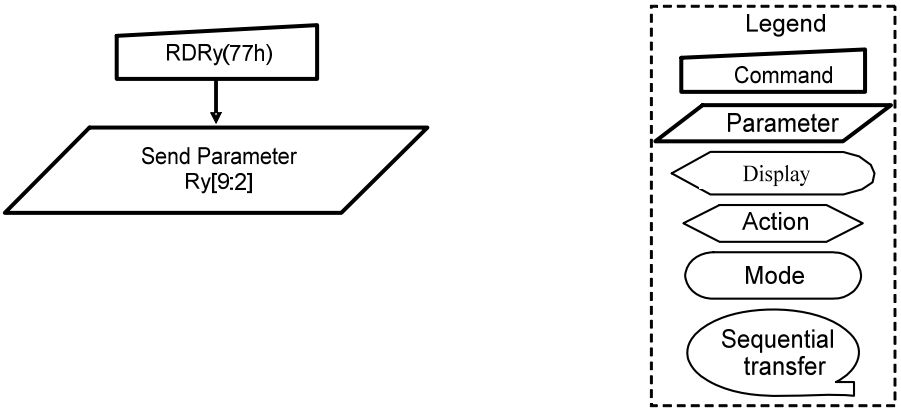
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDGx (7800h): Read Gx**

| 7800H | RDGx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Gx9 | Gx8 | Gx7 | Gx6 | Gx5 | Gx4 | Gx3 | Gx2 | 00 |
| Description | This command returns the Gx bit (Gx[9:2]) of green color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

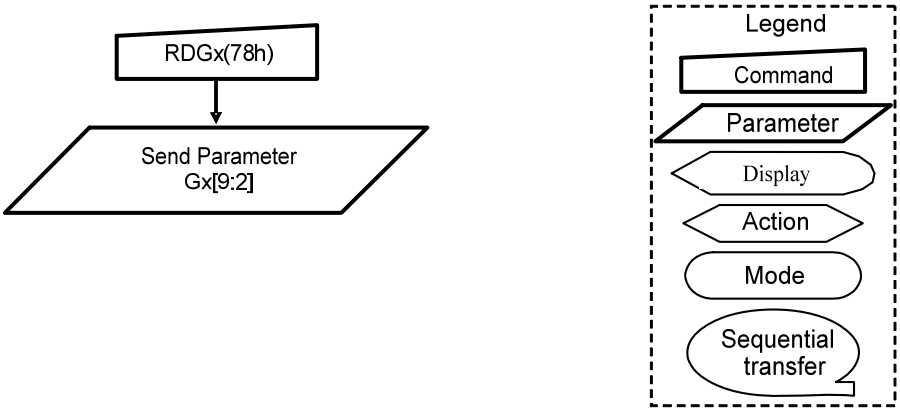
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDGy (7900h): Read Gy**

| 7900H | RDGy | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 79 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Gy9 | Gy8 | Gy7 | Gy6 | Gy5 | Gy4 | Gy3 | Gy2 | 00 |
| Description | This command returns the Gy bit (Gy[9:2]) of green color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

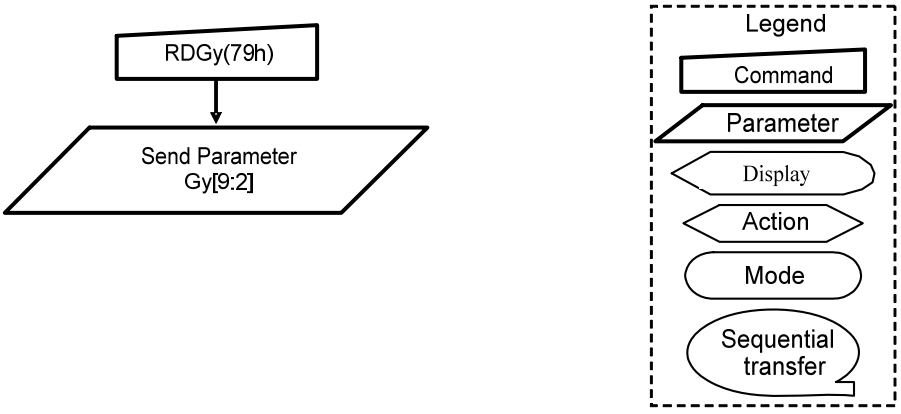
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDBALB (7A00h): Read Red/Green Low Bits**

| 7A00H | RDBALB | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Bx1 | Bx0 | By1 | By0 | Ax1 | Ax0 | Ay1 | Ay0 | 00 |
| Description | This command returns the lowest bits of blue and A color characteristic.<br>Blue: Bx and By<br>A: Ax and Ay | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

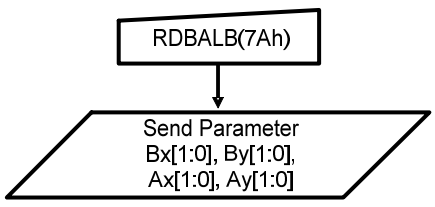
Register Availability

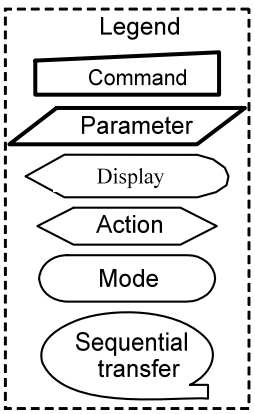
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDBx (7B00h): Read Rx**

| 7B00H | RDBx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Bx9 | Bx8 | Bx7 | Bx6 | Bx5 | Bx4 | Bx3 | Bx2 | 00 |
| Description | This command returns the Bx bit (Bx[9:2]) of blue color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

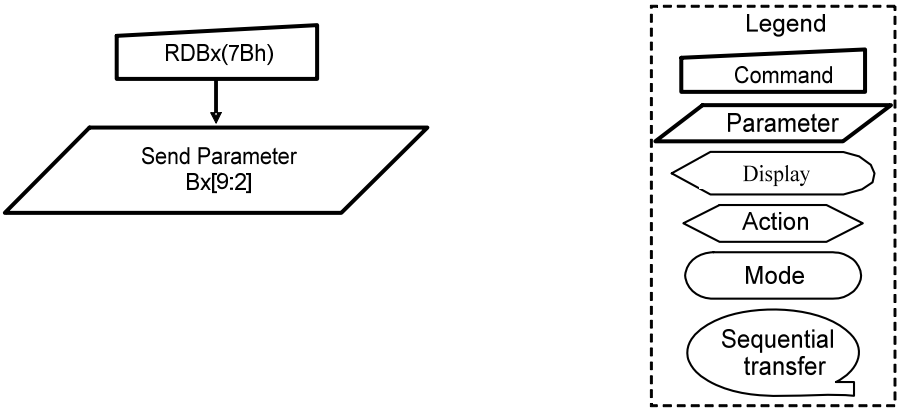
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDBy (7C00h): Read By**

| 7C00H | RDBy | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | By9 | By8 | By7 | By6 | By5 | By4 | By3 | By2 | 00 |
| Description | This command returns the By bit (By[9:2]) of blue color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

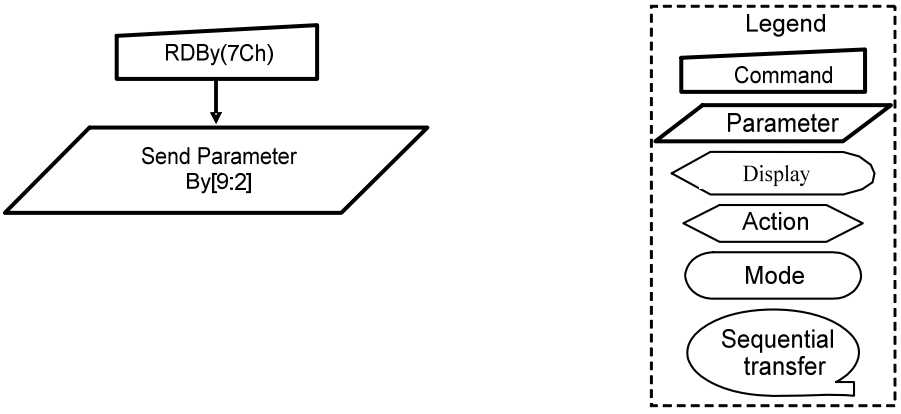
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDAx (7D00h): Read Ax**

| 7D00H | RDAx | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7D |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Ax9 | Ax8 | Ax7 | Ax6 | Ax5 | Ax4 | Ax3 | Ax2 | 00 |
| Description | This command returns the Ax bit (Ax[9:2]) of A color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

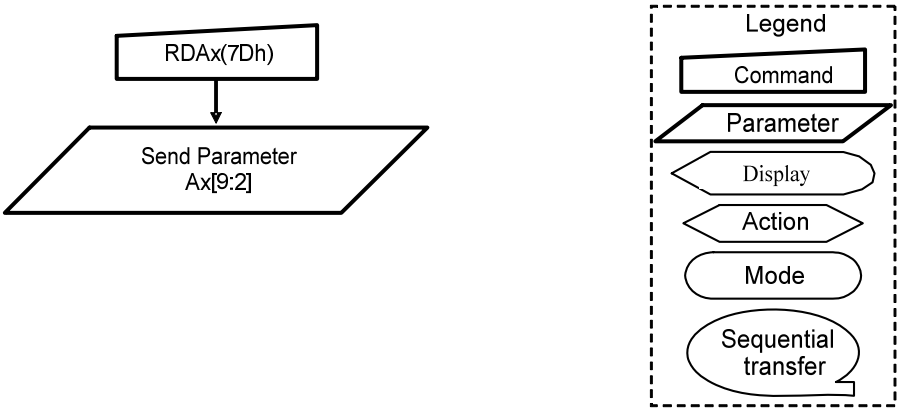
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDAy (7E00h): Read Ay**

| 7E00H | RDAy | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | x | Ay9 | Ay8 | Ay7 | Ay6 | Ay5 | Ay4 | Ay3 | Ay2 | 00 |
| Description | This command returns the Ay bit (Ay[9:2]) of A color characteristic. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

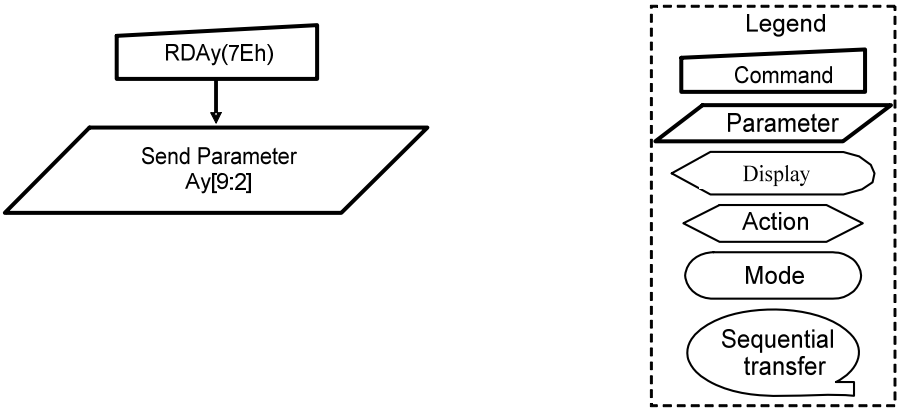
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDDDBS(A1h) : Read_DDB_Start (A1h)**

| A1H | RDDDBS(Read_DDB_Start) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | ID1[15] | ID1[14] | ID1[13] | ID1[12] | ID1[11] | ID1[10] | ID1[9] | ID1[8] | 00 |
| 3rd parameter | 1 | ↑ | 1 | xx | ID1[7] | ID1[6] | ID1[5] | ID1[4] | ID1[3] | ID1[2] | ID1[1] | ID1[0] | 00 |
| 4th parameter | 1 | ↑ | 1 | xx | ID2[15] | ID2[14] | ID2[13] | ID2[12] | ID2[11] | ID2[10] | ID2[9] | ID2[8] | 00 |
| 5th parameter | 1 | ↑ | 1 | xx | ID2[7] | ID2[6] | ID2[5] | ID2[4] | ID2[3] | ID2[2] | ID2[1] | ID2[0] | 00 |
| 6th parameter | 1 | ↑ | 1 | xx | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |
| Description | 1st parameter: Dummy read<br>2nd parameter: Supplier ID code<br>3rd parameter: Supplier ID code<br>4th parameter: Module ID<br>5th parameter: Module ID | | | | | | | | | | | | |
| Restriction | | | | | | | | | | | | | |
| Register Availability | | | | | | | | | | | | | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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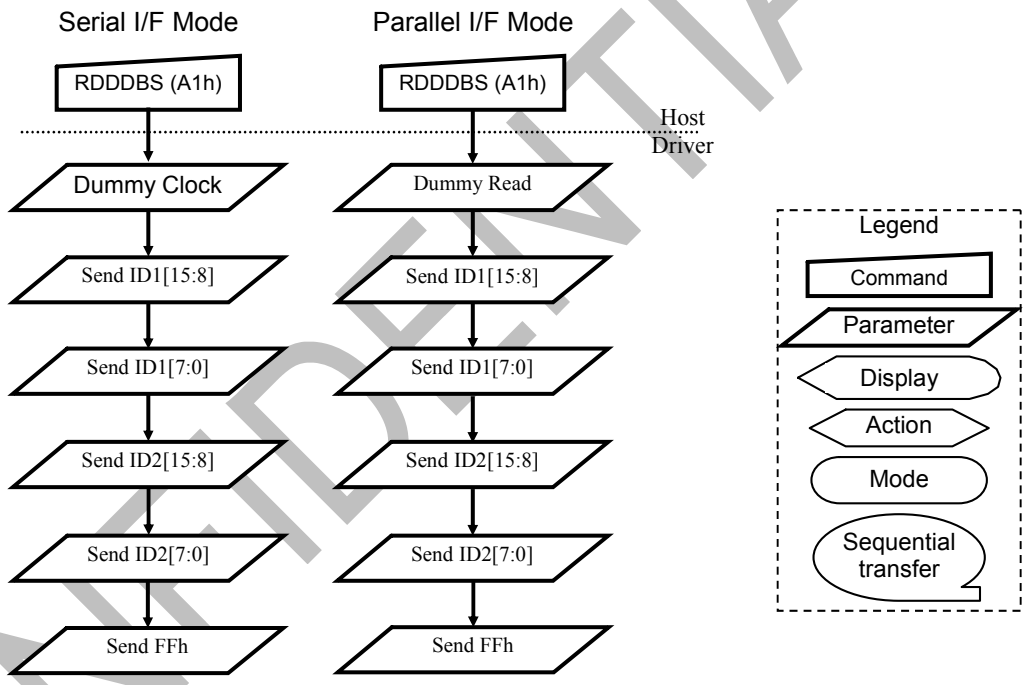
**Default**

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

**Flow Chart**

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**RDDDBC(A800h) : Read DDB Contin**

| A800H | RDDDBC | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | ID1[15] | ID1[14] | ID1[13] | ID1[12] | ID1[11] | ID1[10] | ID1[9] | ID1[8] | 00 |
| 3rd parameter | 1 | ↑ | 1 | xx | ID1[7] | ID1[6] | ID1[5] | ID1[4] | ID1[3] | ID1[2] | ID1[1] | ID1[0] | 00 |
| 4th parameter | 1 | ↑ | 1 | xx | ID2[15] | ID2[14] | ID2[13] | ID2[12] | ID2[11] | ID2[10] | ID2[9] | ID2[8] | 00 |
| 5th parameter | 1 | ↑ | 1 | xx | ID2[7] | ID2[6] | ID2[5] | ID2[4] | ID2[3] | ID2[2] | ID2[1] | ID2[0] | 00 |
| 6th parameter | 1 | ↑ | 1 | xx | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF |

| | |
|---|---|
| Description | This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command.<br>*Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.*<br>*Note: For use example,*<br>*1. Set maximum return packet size=3*<br>*2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]*<br>*3. Read* 0xA8*, return 2 bytes MID[15:8] and 0xFF* |
| Restriction | A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

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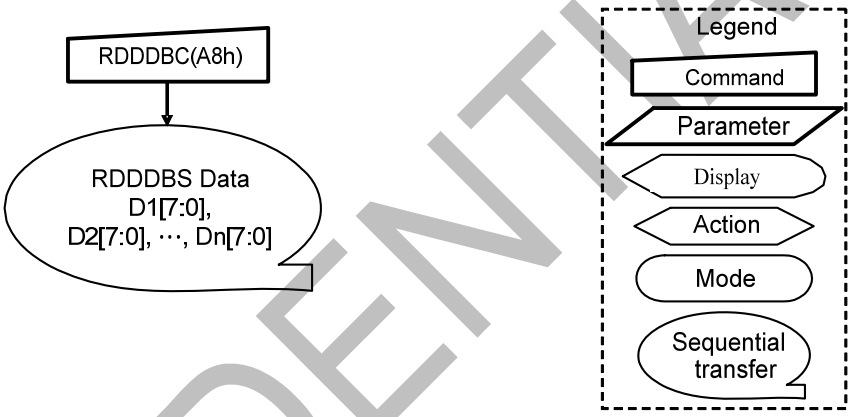
Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

Flow Chart

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**RDFCS(AA00h) : Read First Checksum**

| AA00H | RDFCS | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | AA |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | FCS7 | FCS6 | FCS5 | FCS4 | FCS3 | FCS2 | FCS1 | FCS0 | 00 |
| Description | This command returns the first checksum what has been calculated from “User Command Set” area registers (not include “Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done. | | | | | | | | | | | | |
| Restriction | It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

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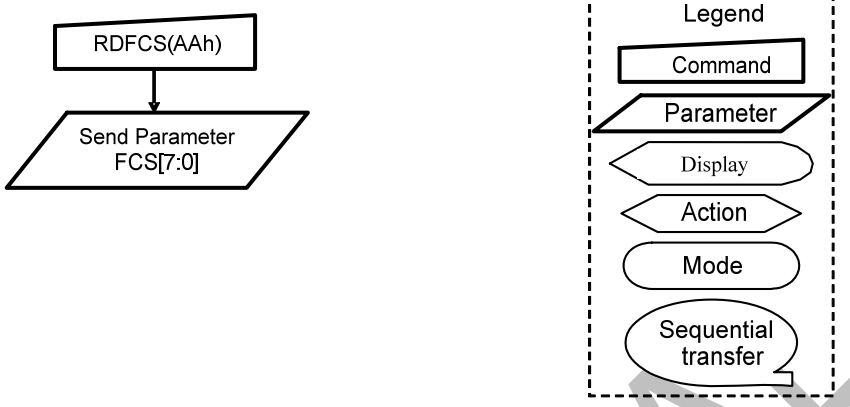
| | |
|---|---|
| Flow Chart |  |



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**RDCCS(AF00h) : Read Continue Checksum**

| AF00H | RDCCS | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | AF |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | CCS7 | CCS6 | CCS5 | CCS4 | CCS3 | CCS2 | CCS1 | CCS0 | 00 |
| Description | This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done. | | | | | | | | | | | | |
| Restriction | It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value in the first time. | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

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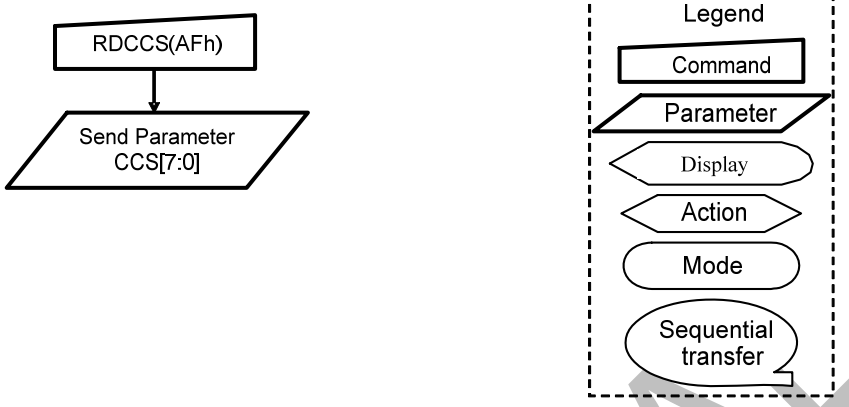
| | |
|---|---|
| Flow Chart |  |



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**RDID1(DA00h) : Read ID1**

| DA00H | RDID1 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | 00 |
| Description | This read byte identifies the TFT LCD module's manufacture ID. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

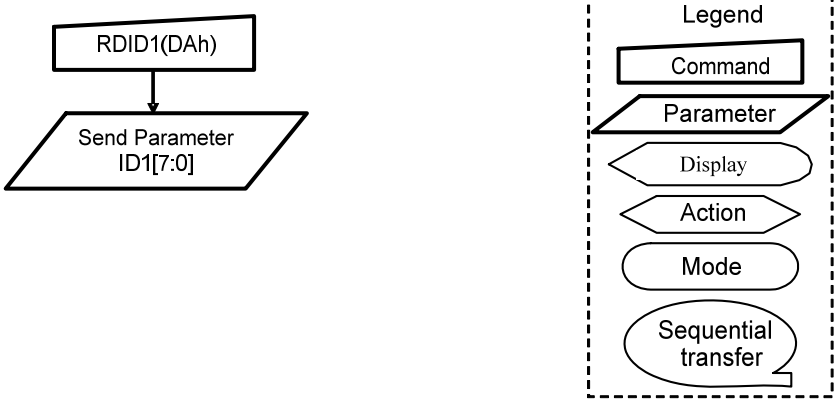
Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| SW Reset | 00h |
| HW Reset | 00h |

Flow Chart

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**RDID2(DB00h) : Read ID2**

| DB00H | RDID2 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | 00 |
| Description | This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications.<br>Parameter Range: ID2 = 80h to FFh | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 80h |
| SW Reset | MTP Value | 80h |
| HW Reset | MTP Value | 80h |

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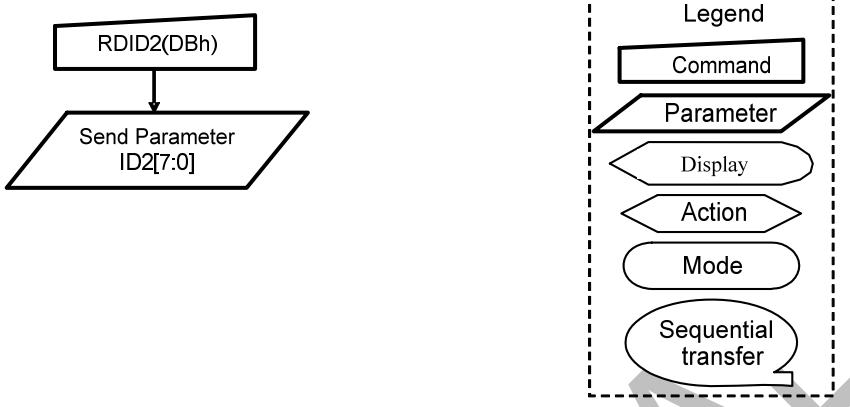
| | |
|---|---|
| Flow Chart |  |



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**RDID3(DC00h) : Read ID3**

| DC00H | RDID3 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DCX | RDX | WRX | D15-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | x | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC |
| 1st parameter | 1 | ↑ | 1 | x | x | x | x | x | x | x | x | x | x |
| 2nd parameter | 1 | ↑ | 1 | xx | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | 00 |
| Description | This parameter read byte identifies the TFT LCD module/driver. | | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | After MTP | Before MTP |
| Power On Sequence | MTP Value | 00h |
| SW Reset | MTP Value | 00h |
| HW Reset | MTP Value | 00h |

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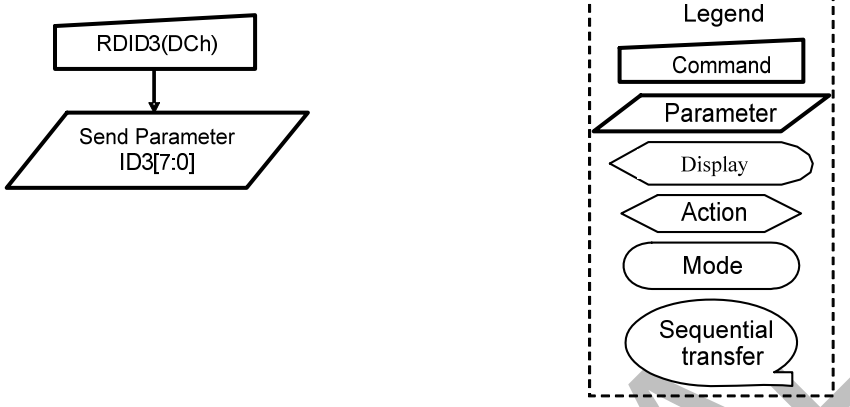
| | |
|---|---|
| Flow Chart |  |



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# 9. Electrical Characteristics

### 9.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM68120 is used out of the absolute maximum ratings, the RM68120 may be permanently damaged. To use the RM68120 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM68120 will malfunction and cause poor reliability.

| item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VDDI | -0.3 ~ + 5.5 | V |
| Power supply voltage | VDDA, VDDB, VDDR, VDDAM | -0.3 ~ + 5.5 | V |
| Supply voltage (Digital) | DVDD, DIOPWR | -0.3 ~ + 2.0 | V |
| Supply voltage (MV) | AVDD-AVSS | -0.3 ~ + 6.6 | V |
| | AVEE-AVSS | -0.3 ~ + 6.6 | V |
| Supply voltage (HV) | VGH - VGLX | -0.3 ~ + 33 | V |
| Input voltage | VIN | -0.3 ~ VDDI+ 0.3 | V |
| Output voltage | VO | -0.3 ~ VDDI+ 0.3 | V |
| Differential input voltage | HSSI_CLK_P/N | -0.3 ~ +1.8 | V |
| | HSSI_DATA0_P/N | | |
| | HSSI_DATA1_P/N | | |
| Operating temperature | Topr | -40 ~ + 85 | °C |
| Storage temperature | Tstg | -55 ~ + 125 | °C |
| Notes:<br>If one of the above itemsis exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range. | | | |

### 9.2 ESD Protection Level

| Model | Test Condition | Level |
|---|---|---|
| Human Body Mode | R = 1.5 kohm / C = 100 pF | > 2.5KV |
| Machine Mode | R = 0 ohm / C = 200 pF | > 250V |

### 9.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

### 9.4 Light Seneitivity

The operation of the IC will not be materially altered by incident light.

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## 9.5 DC Characteristics

### 9.5.1 Basic Characteristics

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Related Pins |
|---|---|---|---|---|---|---|---|
| Analog Power Supply Voltage | VCI | Operation Voltage | 2.3 | 3.7 | 4.8 | V | Note 1 |
| I/O pin Power Supply Voltage | VDDI | I/O supply voltage | 1.65 | 2.8 | 3.3 | V | Note 1 |
| | VDDIL | I/O supply voltage | 1.1 | 1.2 | 1.3 | V | Note 1 |
| | | | | | | | |
| Logic High level input voltage | VIH | VDDI = 1.65V ~ 3.3V | 0.7* VDDI | - | VDDI | V | Note 2 |
| Logic Low level input voltage | VIL | VDDI = 1.65V ~ 3.3V | 0.0 | - | 0.3* VDDI | V | Note 2 |
| Logic High level Output voltage | VOH | Iout = -1 mA | 0.8* VDDI | - | VDDI | V | Note 2 |
| Logic Low level Output voltage | VOL | Iout = +1 mA | 0.0 | - | 0.2* VDDI | V | Note 2 |
| Logic High level input current (Except MIPI/MDDI) | IIHD | Vin=0~VDDI | | | 1 | uA | Note 2 |
| Logic Low level input current (Except MIPI/MDDI) | IILD | Vin=0~VDDI | -1 | | | uA | Note 2 |
| Logic High level input current (MIPI/MDDI) | IIHD | Vin=0~VDDAM | | | 1 | uA | Note 2 |
| Logic Low level input current (MIPI/MDDI) | IILD | Vin=0~VDDAM | -1 | | | uA | Note 2 |
| | | | | | | | |
| AVDD booster voltage | AVDD | | 4.5 | | 6.5 | V | |
| AVEE booster voltage | AVEE | | -6.5 | | -4.5 | V | |
| VCL booster voltage | VCL | | -2.5 | | -4 | V | |
| VGH booster voltage | VGH | | AVDD +VDDB | | 2AVDD -AVEE | V | |
| VGLX booster voltage | VGLX | | AVEE +VCL | | 2AVEE -AVDD | V | |
| Voltage difference between VGH and VGLX | VGHL | \|VGH-VGLX\| | | | 30 | V | |
| | | | | | | | |
| VCOM Amplitude voltage | VCOM | | -3.5 | | 0.0 | V | |
| | | | | | | | |
| Gamma reference voltage | VGMP | | 3.0 | | 6.3 | V | Note 3 |
| | VGSP | | 0.0 | | 3.7 | V | Note 3 |
| | VGMN | | -6.3 | | -3.0 | V | Note 3 |
| | VGSN | | -3.7 | | 0.0 | V | Note 3 |
| Output offset voltage | $V_{OFSET}$ | | | | 45 | mV | Note 3 |
| Output deviation voltage | $V_{DEV}$ | Sout≥4.0V, Sout≤1.0V | | | 20 | mV | Note 3 |
| | | 1.0V<Sout<4.0V | | | 10 | mV | Note 3 |

*Notes: 1. VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSSI=VSS=DVSS=0V, VDD means VDDA, VDDR, VDDB, VDDIM, VDDAM and VSS means VSSA, VSSR, VSSB, AVSS, VSSIM, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level.*

*2. TA = -30 to 85 ℃.*

*3. Source channel loading =5KΩ+55pF/channel.*

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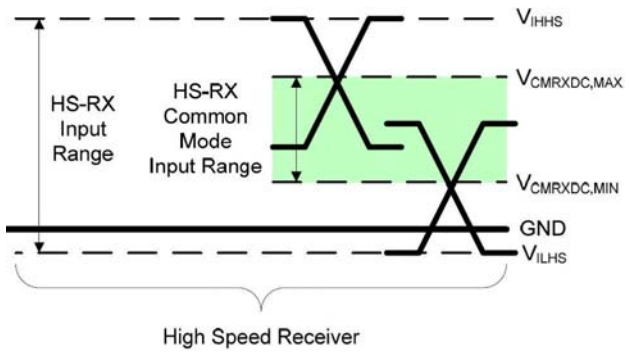
### 9.5.2 MIPI Characteristics

**High-Speed Receiver Specification**

DC Specifications




| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| VCMRX(DC) | Common-mode voltage HS receive mode | 70 | | 330 | mV | 1,2 |
| VIDTH | Differential input high threshold | | | 70 | mV | |
| VIDTL | Differential input low threshold | -70 | | | mV | |
| VIHHS | Single-ended input high voltage | | | 460 | mV | 1 |
| VILHS | Single-ended input low voltage | -40 | | | mV | 1 |
| ZID | Differential input impedance | 80 | 100 | 125 | Ω | |

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

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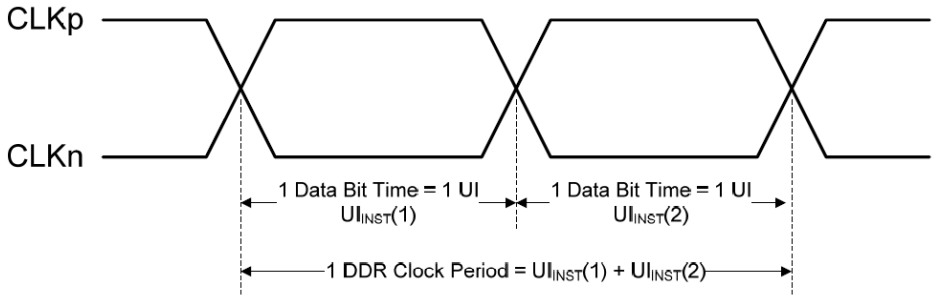
### Forward high speed transmissions

DDR Clock Definition




| Clock Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | | | 12.5 | ns | 1,2 |

Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Data to Clock Skew [measured at transmitter] | $T_{SKEW[TX]}$ | -0.15 | | 0.15 | $UI_{INST}$ | 1 |
| Data to Clock Setup Time [receiver] | $T_{SETUP[RX]}$ | 0.15 | | | $UI_{INST}$ | 2 |
| Clock to Data Hold Time [receiver] | $T_{HOLD[RX]}$ | 0.15 | | | $UI_{INST}$ | 2 |

Notes:

1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of 0.3*UIINST

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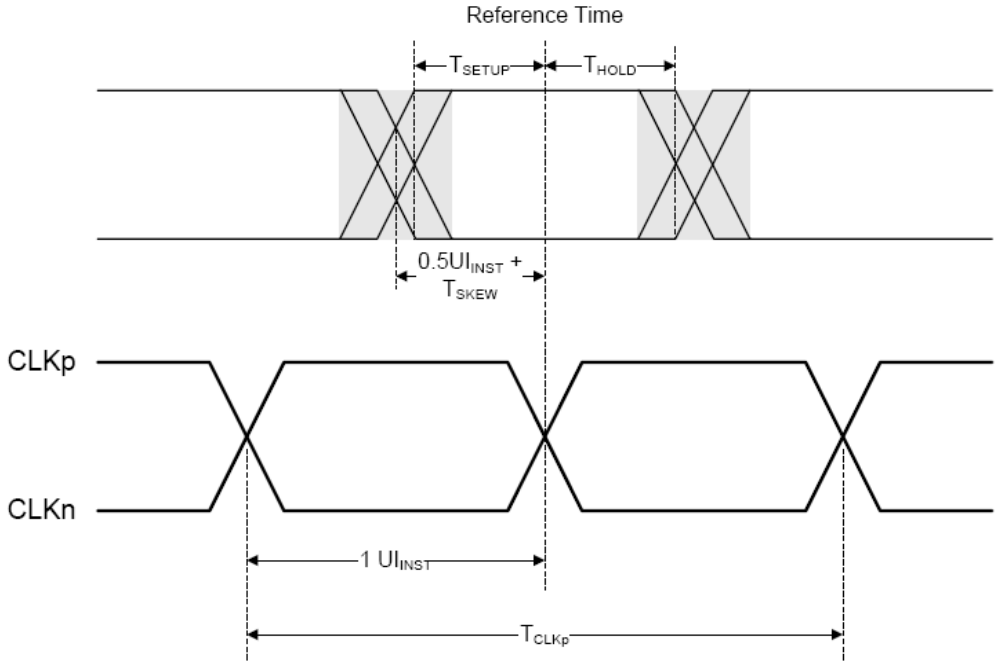
**Data to Clock Timing Definitions**

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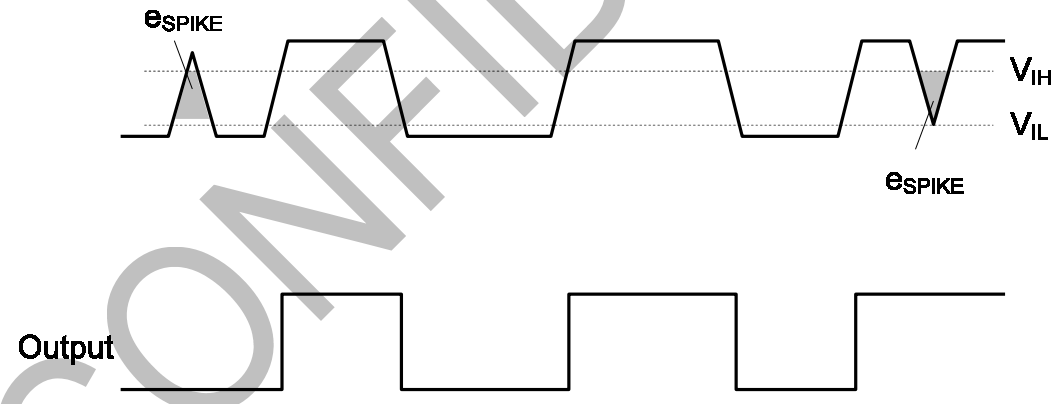
**Low power transceiver specifications**

| Parameters | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Logic high level input voltage | VIHCD | Contention Detection (Lane_D0) | 450 | | 1350 | mV |
| Logic low level input voltage | VILCD | Contention Detection (Lane_D0) | 0 | | 200 | mV |
| Logic high level input voltage | VIH-LPRX | LP-Rx (Lane_CK, Lane_D0, Lane_D1) | 880 | - | 1350 | mV |
| Logic low level input voltage | VIL-LPRX | LP-Rx (Lane_CK, Lane_D0, Lane_D1 | 0 | | 550 | mV |
| Logic low level input voltage | VIL-ULPS | LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1) | 0 | | 300 | mV |
| Logic high level input voltage | VOH-LPTX | Contention Detection (Lane_D0) | 1.1 | 1.2 | 1.3 | V |
| Logic low level input voltage | VOL-LPTX | Contention Detection (Lane_D0) | -50 | 0 | 50 | mV |
| eSPIKE(1.2.3) | Fig. 2 | Input pulse rejection | | | 300 | V.ps |

Notes:

- Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
- An impulse less than this will not change the receiver state.
- In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

Input Glitch Rejection of Low Power Receivers as follow.

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### 9.5.3 MDDI Characteristics

Characteristics

| Parameter | Symbol | Conditions | Specification | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Differential input “High” level voltage (hibernation wake-up) | $V_{IT+offset}$ | VT=125mv (MDDI_DATA_P/M) | - | 100 | 125 | mv |
| Differential input “Low” level voltage (hibernation wake-up) | $V_{IT-offset}$ | VT=125mv (MDDI_DATA_P/M) | 75 | 100 | - | mv |
| Differential input “High” level voltage | $V_{IT+}$ | VT=0mv (MDDI_STB_P/M ,MDDI_DATA_P/M) | - | 0 | 50 | mv |
| Differential input “Low” level voltage | $V_{IT-}$ | VT=0mv (MDDI_STB_P/M ,MDDI_DATA_P/M) | -50 | 0 | - | mv |
| Terminal impedance | Zt | - | 80 | - | 125 | ohm |

Note 1) VDDI= 1.65~3.3V, VDD=2.3 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VDD means VDDAM, VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

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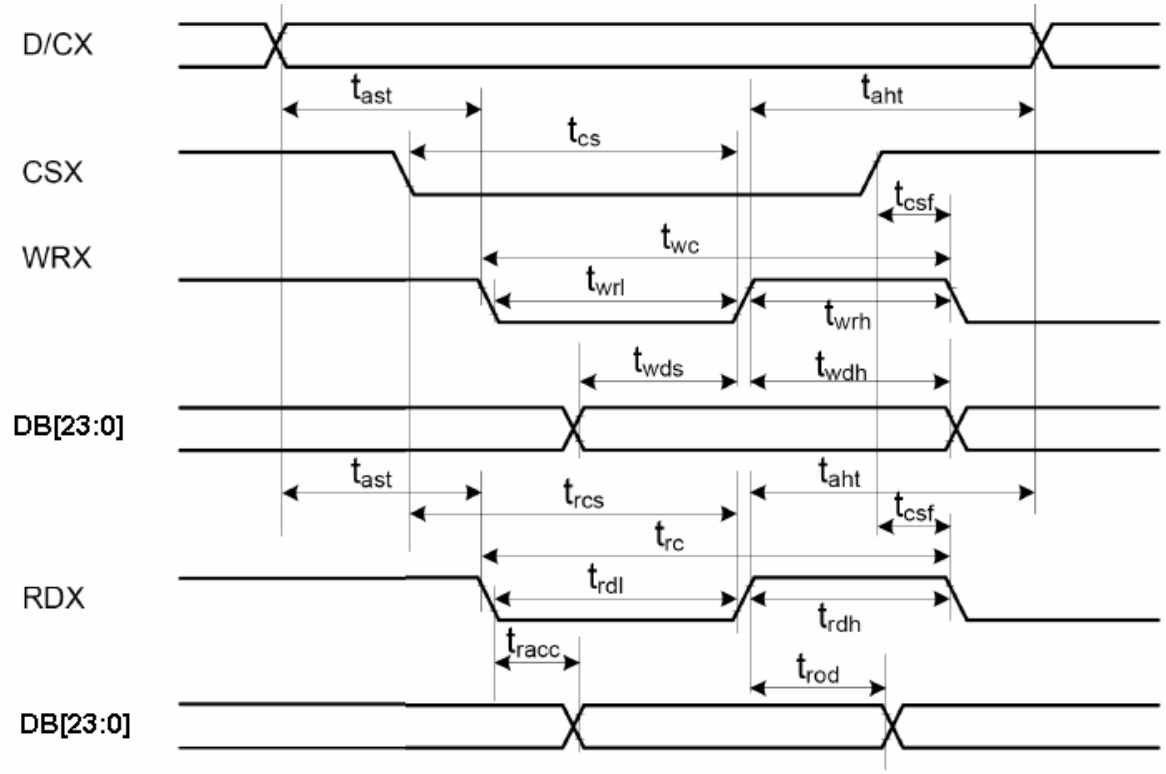
### 9.6 AC Characteristics

#### 9.6.1 Parallel Interface Characteristics (80-Series MCU)




| Signal | Symbol | Parameter | min | max | Unit | Description |
|---|---|---|---|---|---|---|
| DCX | $T_{ast}$ | Address setup time | 10 | - | ns | |
| | $T_{aht}$ | Address hold time (Write/Read) | 2 | - | ns | |
| CSX | $T_{cs}$ | Chip Select setup time (Write) | 20 | - | ns | |
| | $T_{RCS}$ | Chip Select setup time (Read) | 20 | - | ns | |
| | $T_{csf}$ | Chip Select Wait time (Write/Read) | 20 | - | ns | |
| WRX | $T_{wc}$ | Write cycle | 33 | - | ns | |
| | $T_{wrh}$ | Write Control pulse H duration | 15 | - | ns | |
| | $T_{wrl}$ | Write Control pulse L duration | 15 | - | ns | |
| RDX | $T_{rc}$ | Read cycle | 400 | - | ns | Read from frame memory |
| | $T_{rdh}$ | Read Control pulse H duration | 250 | - | ns | |
| | $T_{rdl}$ | Read Control pulse L duration | 150 | - | ns | |
| DB[23:0] | $T_{wds}$ | Write data setup time | 15 | - | ns | |
| | $T_{wdh}$ | Write data hold time | 10 | - | ns | |
| | $T_{racc}$ | Read access time | | 150 | ns | |
| | $T_{rdh}$ | Read output disable time | 5 | - | ns | |

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 4.8V, GND=0V

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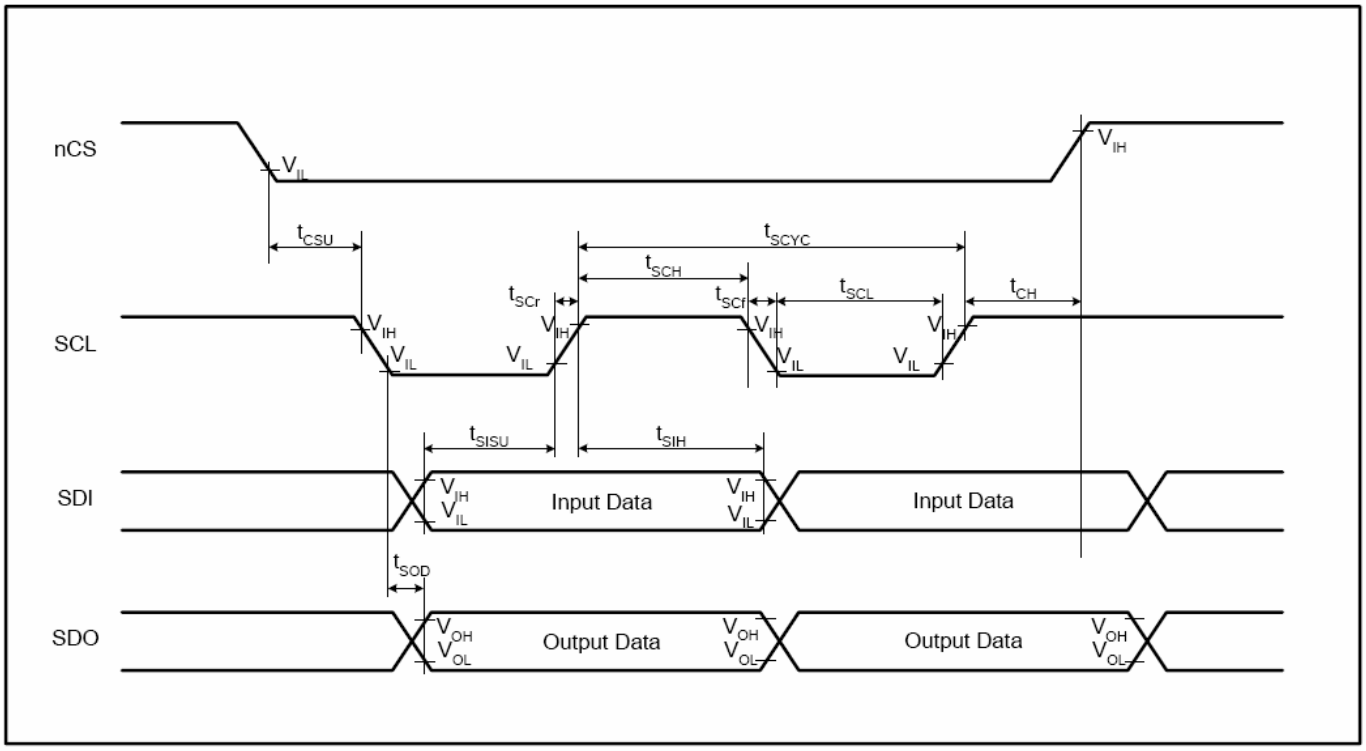
### 9.6.2 Serial Interface Characteristics




| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| SCL | $T_{SCYC}$ | Clock cycle (Write) | 100 | | ns | - |
| | $T_{SCYC}$ | Clock cycle (Read) | 300 | | ns | |
| | $T_{SCH}$ | Clock “H” pulse width (Write) | 40 | | ns | |
| | $T_{SCH}$ | Clock “H” pulse width (Read) | 140 | | ns | |
| | $T_{SCL}$ | Clock “L” pulse width (Write) | 40 | | ns | |
| | $T_{SCL}$ | Clock “L” pulse width (Read) | 140 | | ns | |
| | $T_{SCr}$ | Clock rise time | | 5 | ns | |
| | $T_{SCf}$ | Clock fall time | | 5 | ns | |
| nCS | $T_{CSU}$ | Chip select setup time | 20 | | ns | - |
| | $T_{CH}$ | Chip select hold time | 50 | | ns | |
| SDI | $T_{SISU}$ | Data input setup time | 20 | | ns | - |
| | $T_{SIH}$ | Data input hold time | 20 | | ns | |
| SDO | $T_{SOD}$ | Data output setup time | | 120 | ns | - |
| | $T_{SOH}$ | Data output hold time | 5 | | ns | |

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 4.8V, GND=0V

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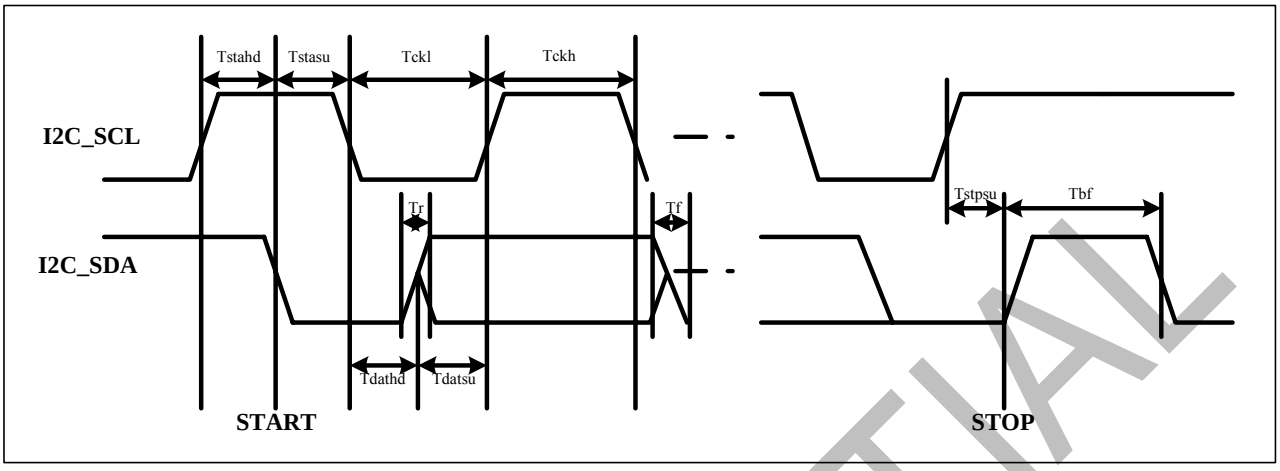
### 9.6.3 I2C Bus Timing Characteristics




| Signal | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| I2C_SCL | Tckl + Tckh | Operate frequency | - | 400 | KHz |
| | Tckl | CLK low | 1300 | - | ns |
| | Tckh | CLK high | 600 | - | ns |
| I2C_SDA | Tr | Data rising time | - | 300 | ns |
| | Tf | Data falling time | - | 300 | ns |
| | Tdathd | Data hold time | 0 | 900 | ns |
| | Tdatsu | Data setup time | 100 | - | ns |
| | Tstahd | Start hold time | 600 | - | ns |
| | Tstasu | Start setup time | 600 | - | ns |
| | Tstpsu | Stop setup time | 600 | - | ns |
| | Tbf | Bus free time | 1300 | - | ns |

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 4.8V, GND=0V

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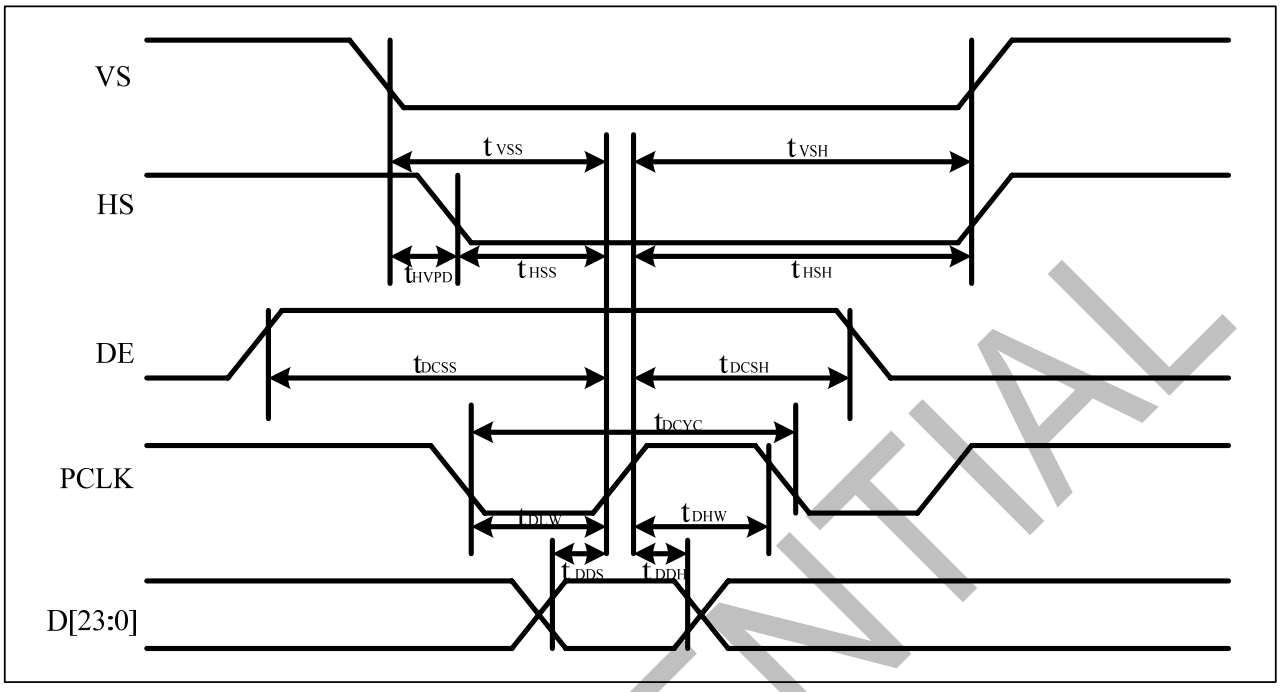
### 9.6.4 RGB Interface Characteristics




| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| VS | $t_{VSS}$ | VS setup time | 10 | - | - | ns |
| | $t_{VSH}$ | VS hold time | 10 | - | - | ns |
| HS | $t_{HSS}$ | HS setup time | 10 | - | - | ns |
| | $t_{HSH}$ | HS hold time | 10 | - | - | ns |
| | $t_{HVPD}$ | HS to VS falling edge | 400 | - | - | ns |
| PCLK | $t_{DCYC}$ | PCLK cycle time | 33 | - | 125 | ns |
| | $t_{DLW}$ | PCLK low pulse width | 11 | - | - | ns |
| | $t_{DHW}$ | PCLK high pulse width | 11 | - | - | ns |
| | $f_{DFREQ}$ | PCLK frequency | 8 | - | 30 | MHz |
| DE | $t_{DCSS}$ | DE setup time | 10 | - | - | ns |
| | $t_{DCSH}$ | DE hold time | 10 | - | - | ns |
| D[23:0] | $t_{DDS}$ | Data setup time | 10 | - | - | ns |
| | $t_{DDH}$ | Data hold time | 10 | - | - | ns |

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 4.8V, GND=0V

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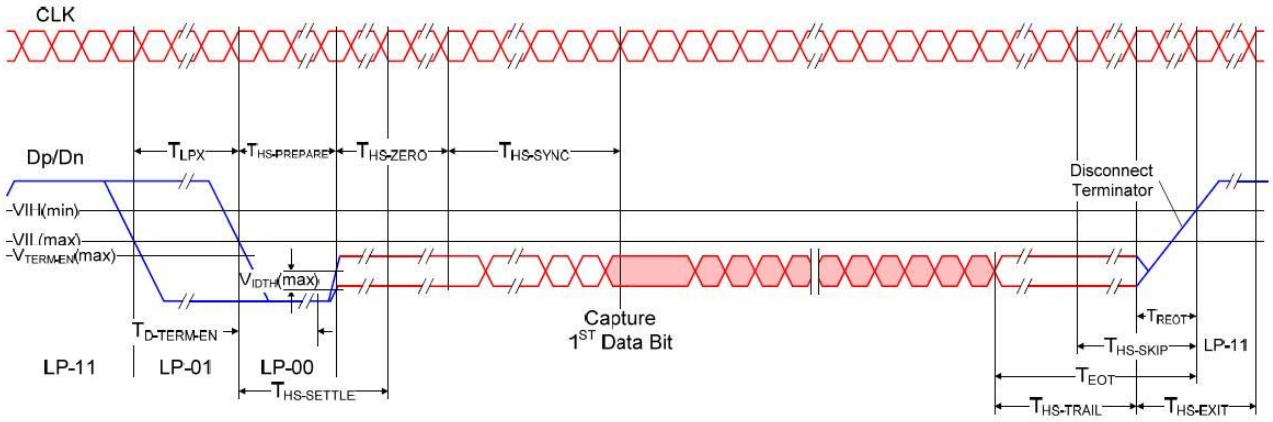
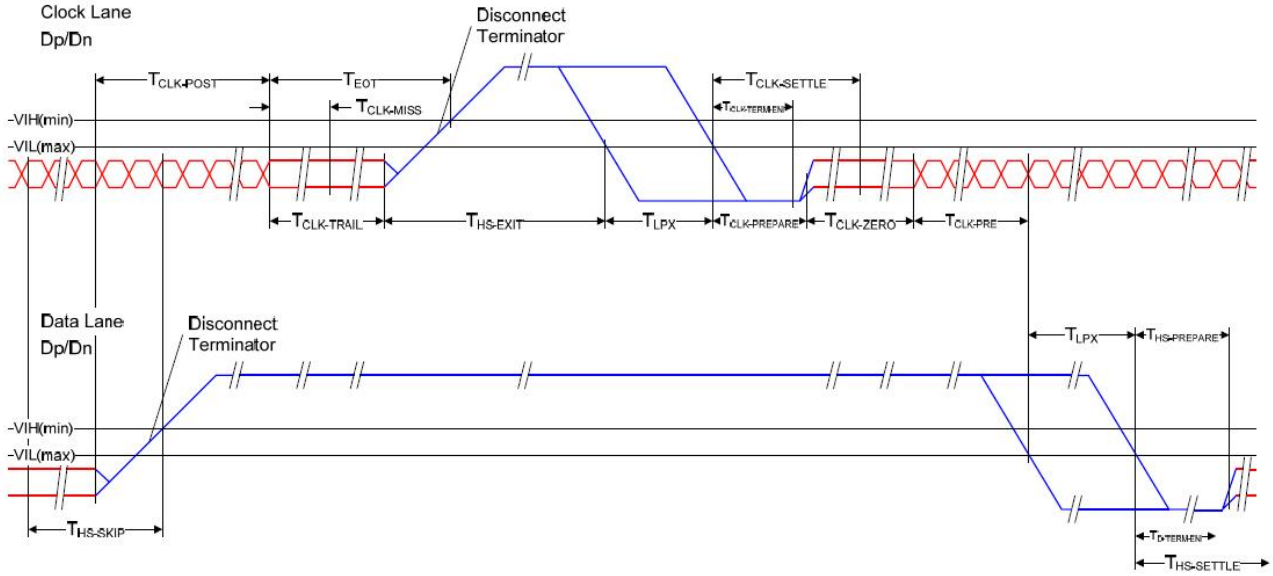
### 9.6.5 DSI Timing Characteristics

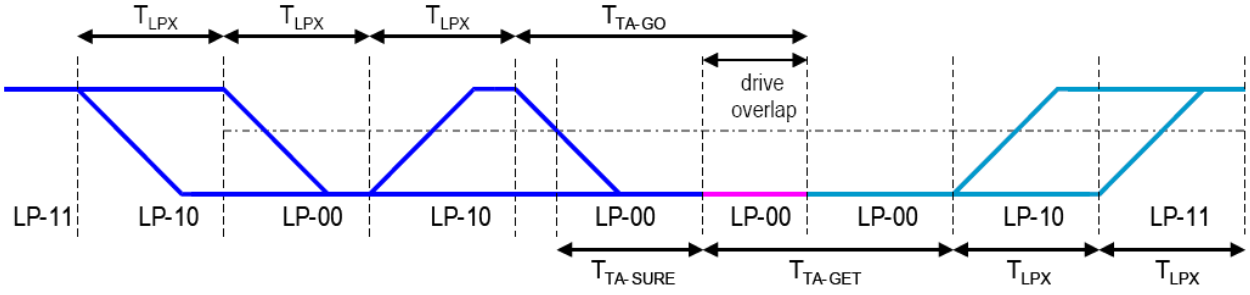
HS Data Transmission Burst




- HS clock transmission




- Turnaround Procedure

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Timing Parameters:

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 ns + 4*UI | | 85 ns + 6*UI | ns | 5 |
| $T_{HS-PREPARE} + T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 ns + 10*UI | | | ns | 5 |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. | 85 ns + 6*UI | | 145 ns + 10*UI | ns | 6 |
| $T_{HS-SKIP}$ | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | | 55 ns + 4*UI | ns | 6 |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | max( n*8*UI, 60 ns + n*4*UI ) | | | ns | 2, 3, 5 |
| $T_{INIT}$ | See section 5.11. | 100 | | | µs | 5 |
| $T_{LPX}$ | Transmitted length of any Low-Power state period | 50 | | | ns | 4, 5 |
| Ratio $T_{LPX}$ | Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side | 2/3 | | 3/2 | | |
| $T_{TA-GET}$ | Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | 5*$T_{LPX}$ | | | ns | 5 |
| $T_{TA-GO}$ | Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | 4*$T_{LPX}$ | | | ns | 5 |
| $T_{TA-SURE}$ | Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX}$ | | 2*$T_{LPX}$ | ns | 5 |
| $T_{WAKEUP}$ | Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS. | 1 | | | ms | 5 |

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{CLK-MISS}$ | Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX. | | | 60 | ns | 1, 6 |
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$. | 60 ns + 52*UI | | | ns | 5 |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI | 5 |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns | 5 |
| $T_{CLK-SETTLE}$ | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$. | 95 | | 300 | ns | 6 |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | Time for Dn to reach $V_{TERM-EN}$ | | 38 | ns | 6 |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns | 5 |
| $T_{CLK-PREPARE} + T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns | 5 |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | Time for Dn to reach $V_{TERM-EN}$ | | 35 ns + 4*UI | | 6 |
| $T_{EOT}$ | Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst. | | | 105 ns + n*12*UI | | 3, 5 |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | | | ns | 5 |

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NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then max( a, b ) = a otherwise max( a, b ) = b
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
4. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

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| Parameter | Description | | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| $T_{RLP}/T_{FLP}$ | 15%-85% rise time and fall time | | | | 25 | ns | 1 |
| $T_{REOT}$ | 30%-85% rise time and fall time | | | | 35 | ns | 1, 5, 6 |
| $T_{LP-PULSE-TX}$ | Pulse width of the LP exclusive-OR clock | First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state | 40 | | | ns | 4 |
| | | All other pulses | 20 | | | ns | 4 |
| $T_{LP-PER-TX}$ | Period of the LP exclusive-OR clock | | 90 | | | ns | |
| $\delta V/\delta t_{SR}$ | Slew rate @ $C_{LOAD}$ = 0pF | | | | 500 | mV/ns | 1, 3, 7, 8 |
| | Slew rate @ $C_{LOAD}$ = 5pF | | | | 300 | mV/ns | 1, 3, 7, 8 |
| | Slew rate @ $C_{LOAD}$ = 20pF | | | | 250 | mV/ns | 1, 3, 7, 8 |
| | Slew rate @ $C_{LOAD}$ = 70pF | | | | 150 | mV/ns | 1, 3, 7, 8 |
| | Slew rate @ $C_{LOAD}$ = 0 to 70pF (Falling Edge Only) | | 30 | | | mV/ns | 1, 2, 3 |
| | Slew rate @ $C_{LOAD}$ = 0 to 70pF (Rising Edge Only) | | 30 | | | mV/ns | 1, 3, 9 |
| | Slew rate @ $C_{LOAD}$ = 0 to 70pF (Rising Edge Only) | | 30 – 0.075 * ($V_{O,INST}$ – 700) | | | mV/ns | 1, 10, 11 |
| $C_{LOAD}$ | Load capacitance | | 0 | | 70 | pF | 1 |

NOTE:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the Lane.

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7. This value represents a corner point in a piecewise linear curve.
8. When the output voltage is in the range specified by VPIN(absmax).
9. When the output voltage is between 400 mV and 700 mV.
10. Where $V_{O,INST}$ is the instantaneous output voltage, VDP or VDN, in millivolts.
11. When the output voltage is between 700 mV and 930 mV.

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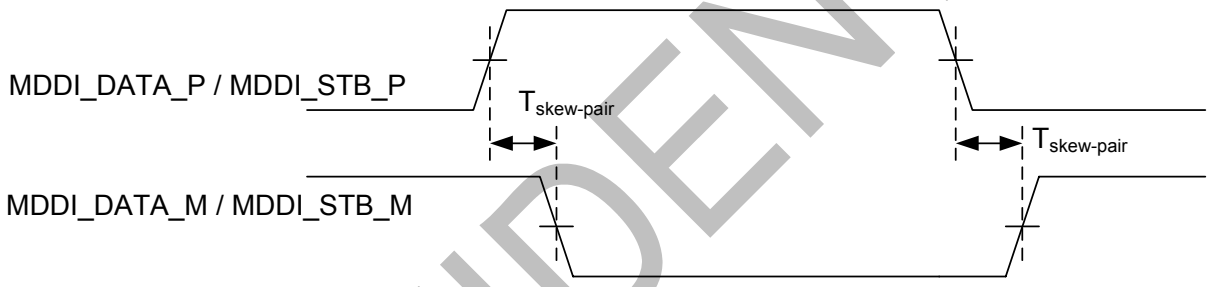
### 9.6.6 MDDI Timing Characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

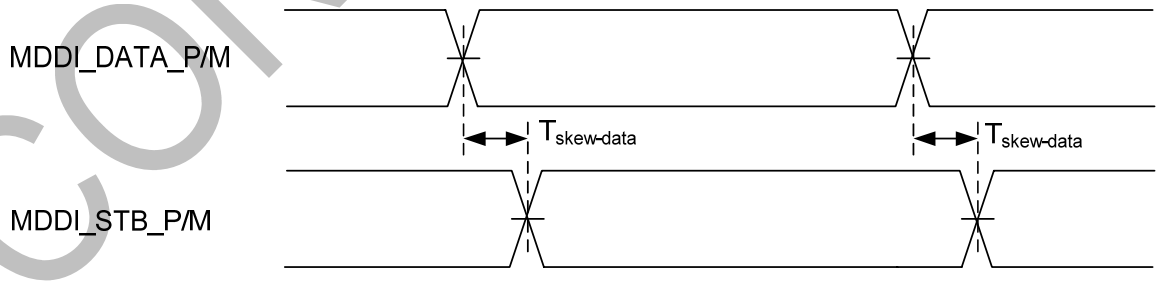
| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| MDDI_STB_P/M<br>MDDI_DATA_P/M | 1/Tbit | Data transfer rate | - | 384 | 450 | Mbps |
| MDDI_STB_P/M<br>MDDI_DATA_P/M | \|Tskew-pair\| | Differential transfer input skew | - | - | 0.05 | ns |
| MDDI_STB_P/M<br>MDDI_DATA_P/M | \|Tskew-data\| | Data/Strobe input skew | - | - | 0.3 | ns |

Note) MDDI_DATA_P/M = MDDI_DATA0_P/M and MDDI_DATA1_P/M.

Skew between MDDI positive and negative signal pair




Skew between MDDI_DATA_P/N and MDDI_STB_P/M

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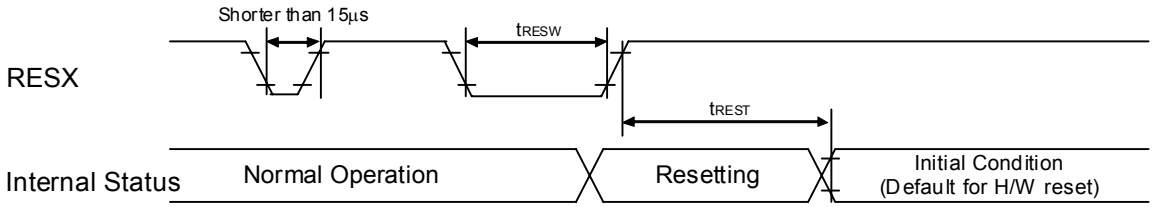
### 9.6.7 Reset Timing




Reset input timing:

IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

| Symbol | Parameter | Related Pins | MIN | TYP | MAX | Note | Unit |
|---|---|---|---|---|---|---|---|
| $t_{RESW}$ | *1) Reset low pulse width | RESX | 15 | - | - | - | μs |
| $t_{REST}$ | *2) Reset complete time | - | - | - | 5 | When reset applied during Sleep in mode | ms |
| | | - | | - | 120 | When reset applied during Sleep out mode | ms |

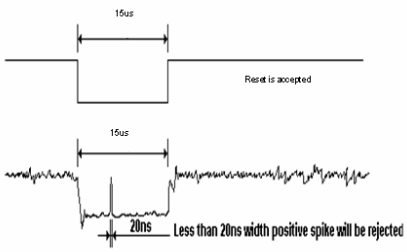
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5μs | Reset Rejected |
| Longer than 15μs | Reset |
| Between 5μs and 15μs | Reset starts<br>(It depends on voltage and temperature condition.) |

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:




Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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